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Temperature Sensitivity Assessment of Nonlinear Channel Tunnel Field-Effect Transistor for Raised Efficiency and Reliability in Nanoscale Electronics

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Abstract: This article presents a thorough assessment of linearity for the Dual Metal Step Channel Heterojunction Negative Capacitance Double Gate Tunnel Field Effect Transistor (SC-HDM-TFET) for the temperature range of 200K to 500K. The SC-HDM-TFET's special dual metal gate, step channel and heterojunction provides better electrostatic control and increased tunneling efficiency. However temperature changes can considerably stimulus the mobility of the carriers, band-to-band tunneling (BTBT) rates by causing 2nd and 3rd order harmonic distortion (HD2 & HD3), intermodulation distortion (IMD3), and input-referred third-order intercept point (IIP3) and 2nd and 3rd order voltage intercept points (VIP2 & VIP3). Device linearity performance is assessed systematically for the specified range of temperature. SILVACO TCAD-2D is used for the device simulations and focus on the temperature-dependent behavior of the proposed device. From the results it is very clear that the SC-HDM-TFET's dual metal layout and step channel design both work together to reduce thermal deterioration and provide exceptional linearity stability even at elevated temperatures. This study demonstrates the SC-HDM-TFET's resilience for use in demanding thermal conditions, guaranteeing dependable operation in electronic systems of the future.

Keywords: Linearity, Temperature Variation, Sensitivity, Step Channel, TFET

1. Introduction

Exploring novel device designs as potential solutions has been made possible by the challenges related to the scaling of metal oxide semiconductor FET (MOSFET) technology. One of the novel device designs that has attracted a lot of research interest is the tunnel field-effect transistor (TFET), which is based on the peculiar current conduction process of band-to-band tunneling (BTBT). The BTBT mechanism [1-4] is a quantum mechanical phenomenon where charge carriers tunnel through a semiconductor's energy bandgap, allowing current to flow even at low supply voltages. Unlike traditional MOSFETs that rely on thermionic emission, where carriers must surmount a potential barrier, BTBT enables electrons to tunnel from the source's valence band to the channel's conduction band due to an electric field, promoting effective carrier injection. The tunneling probability is crucial to this process and is affected by factors like the electric field at the source-channel junction, the semiconductor's bandgap, and the doping levels. Materials with smaller bandgaps and high dielectric constant gate stacks improve tunneling efficiency, resulting in higher drive currents and better device performance. However, a significant challenge for BTBT-based devices is balancing high ON-current with reduced ambipolar conduction, which can occur due to unintended tunneling at the drain. To overcome these issues, various design approaches, including heterojunction engineering, step-channel structures [4], and negative capacitance [5-9] integration, have been investigated to boost tunneling efficiency while reducing leakage currents, positioning TFETs as promising options for ultra-low-power and high-performance applications. Because of its extremely low leakage current and ability to achieve a subthreshold slope below the traditional limit of 60 mV/dec [10], TFETs are superior to conventional MOSFETs and allow for power supply scalability [11]. To enhance the SS of the device, the concept of negative capacitance can be applied on top of high-k dielectric materials like HfO_2. Fe-FETs take

advantage of the negative capacitance (NC) effect found in ferroelectric materials to enhance gate control, allowing for a subthreshold slope (SS) that is steeper than the 60 mV/dec limit, which is a key limitation in traditional MOSFETs. By integrating a ferroelectric material like silicon-doped HfO_2 into the gate stack, Fe-FETs exhibit internal voltage amplification, leading to a notable decrease in power consumption while still delivering high performance. This characteristic makes Fe-FETs a strong contender for ultra-low-power electronic applications.

Apart from these many advantages, TFET suffer from some key issues such as low ON-current, ambipolarity, short channel effects [12-14], etc. to address these issues, many researchers have done the significant work in this area. Agarwal L. *et al.* [15] have investigated the MDMIS-GAA-JLTFET device, which notably reduced the subthreshold swing (SS) to 15 mV/decade, a value that is considerably lower than the limiting SS. Bitra. J. *et al*. [16] has investigated the JL-TFET, enhancing subthreshold performance and addressing the issue of excessive leakage current, which results in improved device sensitivity. Singh P. *et al.* [17] has examines the UTS-F-TFET and found that the device has produced the better ON-current. Jain G. *et al.* [18] has explored the HD-NSH-TFET and reported significant improvement in SS and ON-current. She has also reported that the device is immune to the temperature variations. Vedvrat *et al.* [19] has reported that the DMG-HD DGTFET device is capable of improving the ON-current and SS whereas suppressed the OFF-current and V_{th} significantly. Several other alternative TFET structures and materials have been also suggested to resolve these issues, which includes the SOI-TFET [20], step structures [21], tapered TFET [22], SiGe Pocket [23], dielectric Modulated [24], oxide-engineered [25], T-shaped [26], Z-shaped TFET [27], I-shaped TFET [28], Vertical TFET [29], and C-shaped TFET [30].

In contrast to MOSFETs, which are susceptible to temperature fluctuations due to a variety of causes [31], TFETs are immune to temperature fluctuations due to the BTBT mechanism, which has been found to be weakly dependent on temperature [32, 33]. Although the temperature-dependent properties of TFETs have already been examined and described in prior studies [34, 35], the effect of temperature on circuit performance has not been covered and requires further analysis. The main incentive is to look into how this temperature invariability benefits the TFET-based circuit design and can provide it an advantage over CMOS circuits, as TFET is said to have superior temperature immunity and stability than MOSFET [36]. The linearity analysis [36, 26, 28, 37] based on temperature variation [28, 29, 30, 38] is very critical for the device performance and this will ensure the usability of the device for high frequency and in low power regime. TFET reportedly has better temperature immunity and stability than MOSFET [35]; thus, the key motivation is to investigate how this temperature invariability is beneficial for the TFET and further for the TFET-based circuit design and can provide an edge over CMOS circuits. The paper is set up this way in this instance. The proposed device (SC-HDM-TFET) and simulation arrangement are covered in detail in Section II. In addition, Section III provides a thorough discussion and summary of all the findings. Section IV summarizes the main findings and overall significance of this research to bring the analysis to a close.

2. Simulation Setup and Device Physics

The Dual Metal Step Channel Heterojunction Negative Capacitance Double Gate Tunnel Field Effect Transistor has been designed to overcome the precincts associated with traditional MOSFETs and TFETs. This device combines a step-channel design, a Si doped HfO_2 (ferroelectric) layer, a Germanium pocket, and a dual-metal along with the double gate to optimize to their full potential to improve I_{ON}/I_{OFF}, SS, and V_{th}. The next section covers the structure of the device (SC-HDM-TFET), simulation setup and operation of the device along with the device physics.

2.1 Device Structure and Setup

Figure 1 (a) and (b) illustrate the cross-sectional view of conventional and proposed TFETs in which source (P^+), channel (P) and drain (N^+) regions each having the thickness of 10 nm and having the length of 20 nm, 30 nm and 20 nm respectively. The dimension of the step is 15 nm to 1 nm and placed adjacent to the drain. High-k oxide (HfO_2) and ferro-layer (Si: HfO_2) is stacked with a thickness of 1 nm and 2 nm respectively. Oxide layer and ferro-layer length is 30 nm each respectively, this enhances the electrostatic control and tunneling efficiency. Both structures utilizes the 3 nm Ge-Pocket with the thickness of 10 nm. The pocket helps in improving the ON-current and reducing the SS also by lowering the energy bands of the devices and hence improve the BTBT rate. This arrangement assist in achieving superior performance in low-power and high-frequency applications, mainly under temperature variations. The devices parameters are shown in table 1.

The proposed device was calibrated with reference [39] to match theoretical models and empirical data, optimizing performance metrics like ON-state current, subthreshold swing, and threshold voltage. Factors like carrier mobility, band-to-band tunneling rates, were adjusted, and HfO_2 thicknesses were adjusted for practicality and the results of the proposed device are verified using SILVACO TCAD simulator and the calibrated graph is presented in figure 2.

The device (SC-HDM-TFET) depicted in figure 1 (b) has a sophisticated architecture and layer structure that improve the carrier transport and electrostatic control through its unique layer configuration.

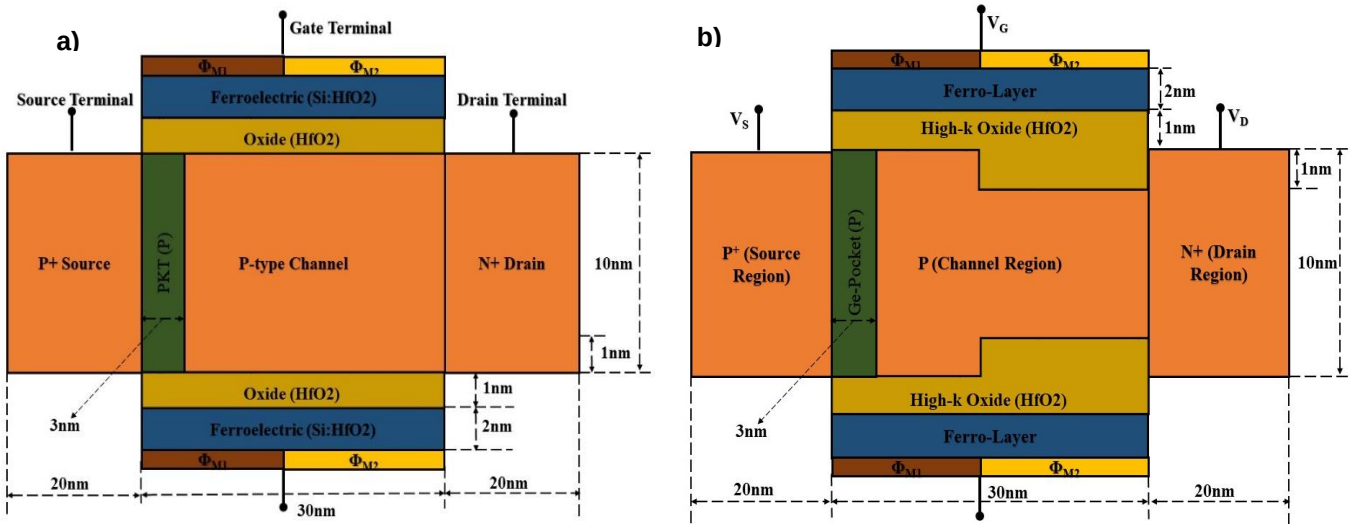

Figure 1. Cross sectional view of (a) HDM-TFET (b) SC-HDM-TFET

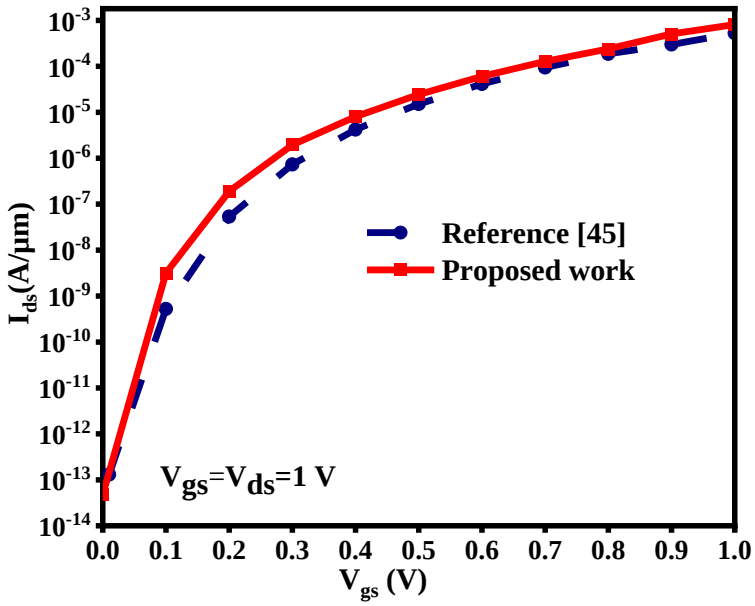

Figure 2. Transfer Characteristics curve for SC-HDM-TFET with the reference data [45]

Along with the high-k oxide layer (HfO_2), the negative capacitance effect improves subthreshold swing, reduces leakage current, and modulates gate electric field. The pocket helps in the channel region, adjacent to the source region, reduces the tunneling barrier width and establishes a precise doping profile to improve band-to-band tunneling (BTBT) and ON-state current. The step in the channel region improves carrier injection and transport by graded energy band alignment, reducing carrier dispersion and increasing mobility. The structure is comprised of a PIN like structure which has highly doped source region and moderately doped drain region and are of P-type and N-type respectively. Whereas, a lightly doped or doping less channel is used as an intrinsic material. The concentration values for the different regions such as source, channel, drain and pocket are 2×10^{20}, 1×10^{15}, 1×10^{17} and 5×10^{20} cm^{-3} respectively. The nonlinearity introduced in the channel helps in reducing the ambipolar effect and OFF-current and enhances the SS of the proposed device. Both the device utilise the dual metal with a work function of 4.2 eV and 4.8 eV.

All the simulations were performed using the SILVACO TCAD simulator leveraging advanced physical models to achieve accurate and realistic results. The simulation relies on the nonlocal band-to-band tunneling (BTBT) model, which calculates tunneling probabilities using energy band diagrams. This model uses experimental data and the Wentzel–Kramer–Brillouin (WKB) approximation to improve precision. The heavily doped source and drain areas are explained by the bandgap narrowing (BGN) concept. Fermi–Dirac statistics precisely replicate charge carrier distribution, while Auger and SRH (Shockley–Read–Hall) recombination models elucidate carrier dynamics.

Table 1. The size and characteristics of the device employed in the simulation

S. No.	Parameter	Symbol	HDM-TFET	SC-HDM-TFET	Unit
1	Drain Voltage	V_{DD}	1.0	1.0 V	V
2	Gate Voltage	V_{GS}	1.0	1.0 V	V
3	Source doping	P^+	2×10^{20}	2×10^{20}	cm-3
4	Channel doping	P	1×10^{15}	1×10^{15}	cm-3
5	Drain doping	N^+	1×10^{17}	1×10^{17}	cm-3
6	Pocket Doping	P^+	5×10^{20}	5×10^{20}	cm-3
7	Source length	L_S	20	20	nm
8	Channel Length	L_C	27	27	nm
9	Drain length	L_D	20	20	nm
10	Pocket length	L_{PKT}	3	3	nm
11	Oxide thickness	t_{ox}	2	2	nm
12	Ferro Material thickness	t_{fe}	2	2	nm
13	Channel thickness	t_C	10	10	nm
14	Step Channel thickness	t_{SC}	NA	1	nm
15	Drain and Source Thickness	$t_D = t_S$	10	10	nm
16	Work Function	Φ_{m1} / Φ_{m2}	4.2 / 4.8	4.2 / 4.8	eV

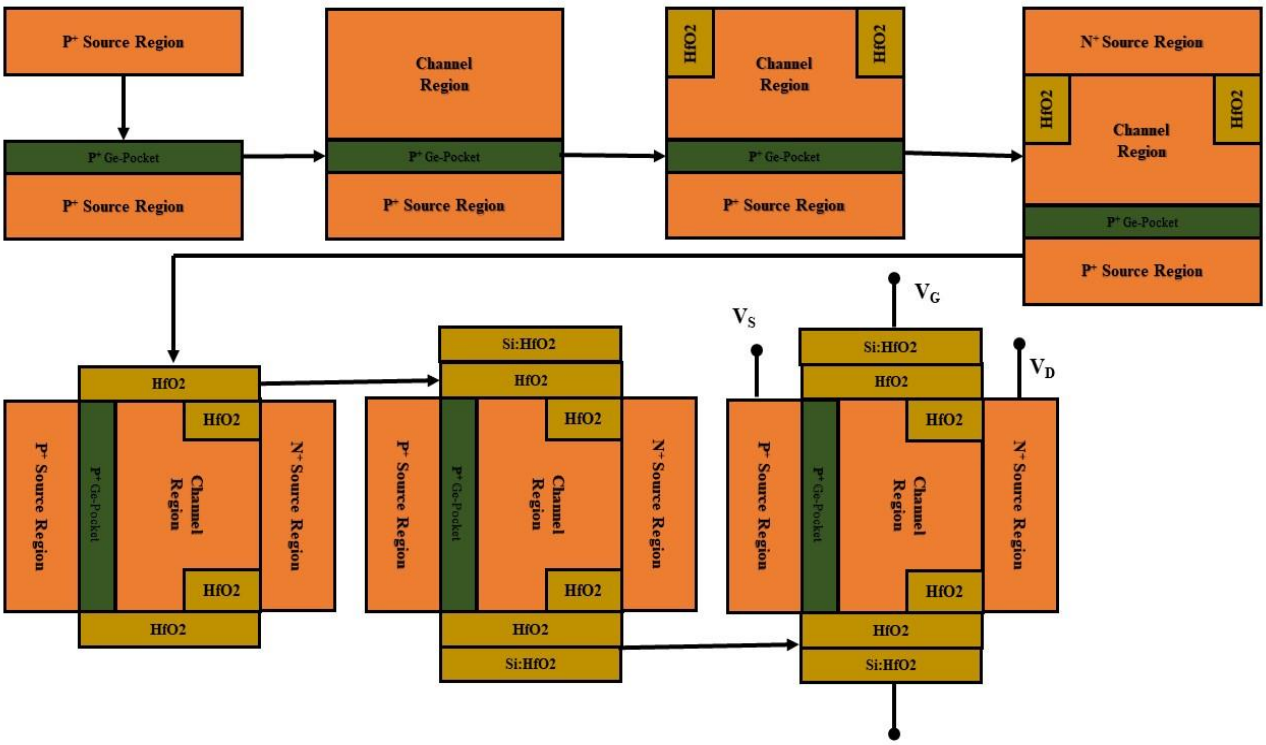

Figure 3. Fabrication steps of SC-HDM-TFET

The simulation uses the FLDMOB (field-dependent mobility) and CONMOB (carrier concentration-dependent mobility) model to account for electric field effects on charge carrier mobility and tests mobility changes due to carrier concentration respectively. When combined, these models explain device behavior, including tunneling, recombination, and carrier transport. By summarizing the simulation device dimensions, Table I makes it easy to evaluate structure performance under different operating situations. This method provides a robust simulation framework for accurate device assessment.

Uniform parameters have been assigned to both the devices such as both the operational voltages are fixed to 1.0V. The Si:HfO2 (used as ferro-layer) material's ferro parameters are has an epsf value of 35.15, P_r of 12.15 × 10^{-6}, Ps of 12.87 × 10^{-6}, and EC of 1.19 × 10^6 [40]. Si:HfO_2's lower dielectric constant of 32.5 reduces fringing [41, 42], making it better choice than SBT and PZT. This process facilitates the reduction of ferroelectric layer thickness [6]. The gate stack ratio shows enhanced efficiency in the scaling process. The MOSFET fabrication procedure indicates compatibility with Si:HfO_2 [43]. Designs must consistently incorporate a substrate–interfacial layer to resolve lattice mismatch issues. The detailed fabrication procedure for the SC-HDM-TFET is shown in figure 3.

The construction of the device start with preparation of the p-type source region on the intrinsic substrate using the ion implantation method. Pocket of Germanium (p-type) is developed using molecular beam epitaxy (MBE) process. P-type channel is fabricated on the pocket using the epitaxy process then after placing the photoresist layer in the selected region and using the photolithography process to define the channel regions which is etched in the next step to create the step in the channel region. Again photoresist is used placed and then using CVD method the drain region (N^+) is fabricated on the channel region. Device is aligned horizontally, photoresist is placed on upper and bottom side of the device leaving the space for the deposition of high-k dielectric material (HfO_2) using the atomic layer deposition (ALD). Sputtering process is used to develop the ferro-layer (Si:HfO_2) on dielectric material. Metal layer are placed using the sputtering method and then after evaporation technique is used for the development of contacts (source, gate and drain).

3. Results

This section provides a comparison of the simulated structures HDM-TFET (conventional device) and SC-HDM-TFET (proposed device), offering an accurate assessment of their physics and functionality. This section examines various factors such as EBD, particle concentration, transfer characteristics, transconductance, and the performances in both analog/RF domains for the two structures.

The energy band diagrams for both devices under thermal equilibrium conditions (V_{gs}=V_{ds}=0.0V), in the OFF-state (V_{gs}=0.0V & V_{ds}=1.0V), and in the ON-state (V_{gs}=V_{ds}=1.0V) are presented in Figures 4(a)–(c) and (d)–(e), respectively. In the thermal equilibrium condition illustrated in figure 4(a), the absence of particle movement between the source and drain regions leads to a significantly large energy band gap between the source and channel regions. This phenomenon results in an equal concentration of particles, as demonstrated in figure 4(d).

Although the particles are capable of traversing the device through traditional methods, Figure 4(b) distinctly demonstrates that the tunneling channel is not accessible, thereby rendering it unfeasible for the particles to advance through the tunneling process. This leads to a modification in the concentration of available particles, as illustrated in figure 4(e).

Figure 4(c) presents the EBD, while Figure 4(e) illustrates the concentration profile. It is clear from both images that the tunneling pathway and, as a result, the concentration of charge particles have markedly enhanced. The feasibility of this phenomenon is contingent solely upon the diminishment of the energy band that exists between the source and the channel. This enables the direct transfer of particles from the source side to the drain side.

Figure 5 depicts the transfer characteristics of the proposed device w.r.t. the conventional device. The graph illustrates the transfer characteristics I_d vs. V_{gs} of SC-HDM-TFET and HDM-TFET, emphasizing the effects of the step-channel and negative capacitance. The SC-HDM-TFET displays a steeper subthreshold slope and a higher drain current, which suggests better tunneling efficiency and improved switching performance. At low Vgs, it maintains minimal leakage current and helps reduce the power consumption, while showing a significant surge in I_d vs. V_{gs} increases, indicating superior on-current. This is evidence that the step-channel design in SC-HDM-TFET significantly boosts device performance compared to traditional HDM-TFET.

Figure 6 shows performance details of transconductance and gain-bandwidth product (GBP) of HDM-TFET, and SC-HDM-TFET, emphasizing the best of SC-HDM-TFET over HDM-TFET because of the stronger carrier transport and the better electrostatics. Figure 7(a) is a graph that reveals the gate-to-source voltage (V_{gs}) dependence of total capacitance (C_{total}), and it is a proof for the presence of negative capacitance, needed for the overall device capacitance minimization for speed. Figure 7(b) gives the transistor parameters f_T and transit time, where SC-HDM-TFET possesses higher f_T and lower transit time, indicating faster switching and response frequency.

The figure 8 (a) illustrates the relationship between TGF (Transconductance Gain Factor) and TFP (Transconductance Frequency Product) w.r.t. V_{gs} for both HDM-TFET and SC-HDM-TFET structures. For both the devices, TGF and TFP initially shows a sharp rise with the increase in Vgs and reached to a peak value, then decrease to a minimum point before rising again, showcasing their switching characteristics and performance.

The I_{on}/I_{off} ratio is depicted in figure 8 (b). The figure clearly reveals that the proposed device has a steeper subthreshold slope and higher on-state current

than the HDM-TFET which signifies the better switching speed and enhancement in the drive capability by the proposed device due to the step channel heterojunction and negative capacitance effects.

The table II shows the comparison of DC and analog parameters for the conventional and the proposed device.

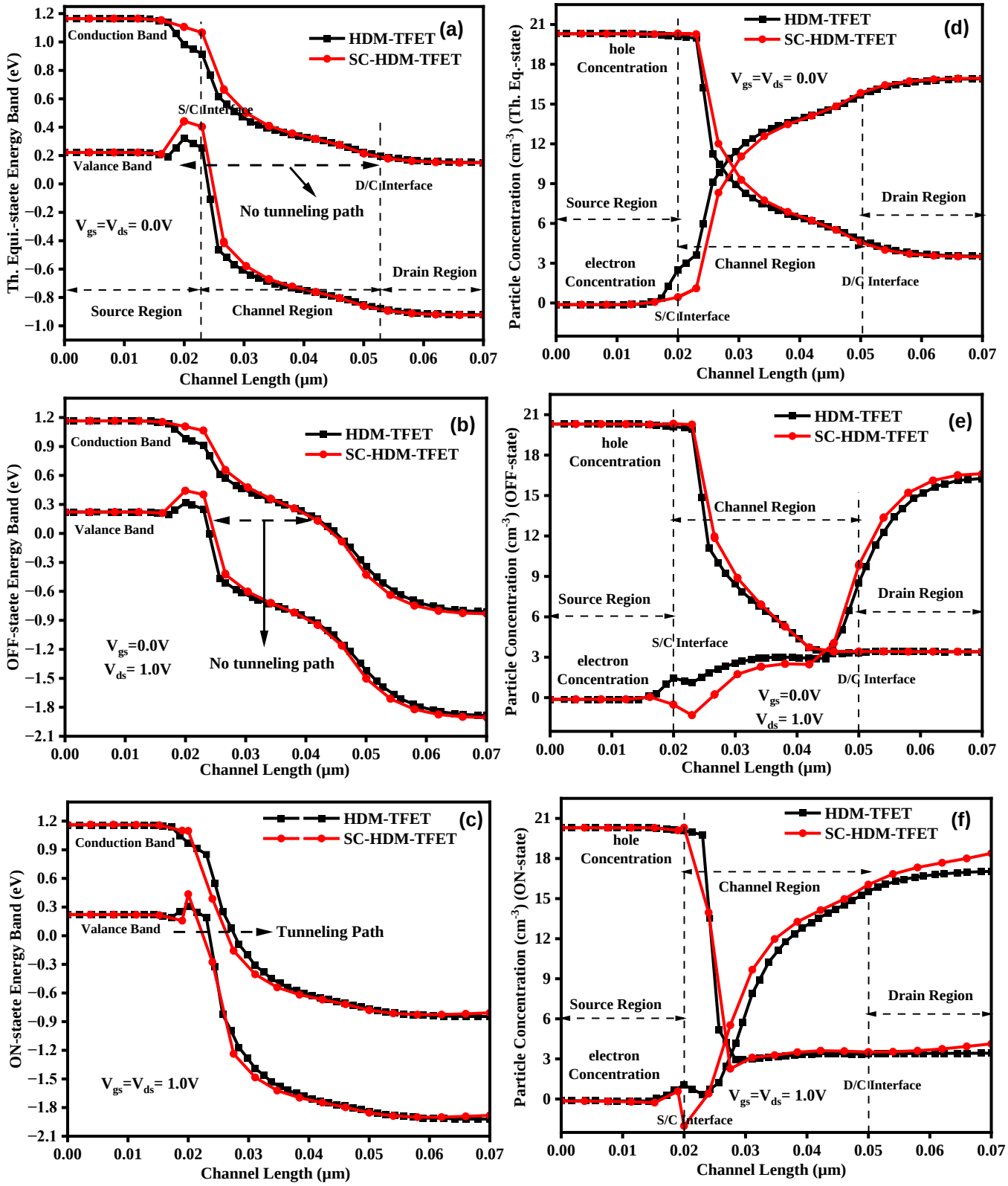

Figure 4. shows the EBD from (a) – (c) and concentration (d) – (e) for HDM-TFET & SC- HDM-TFET

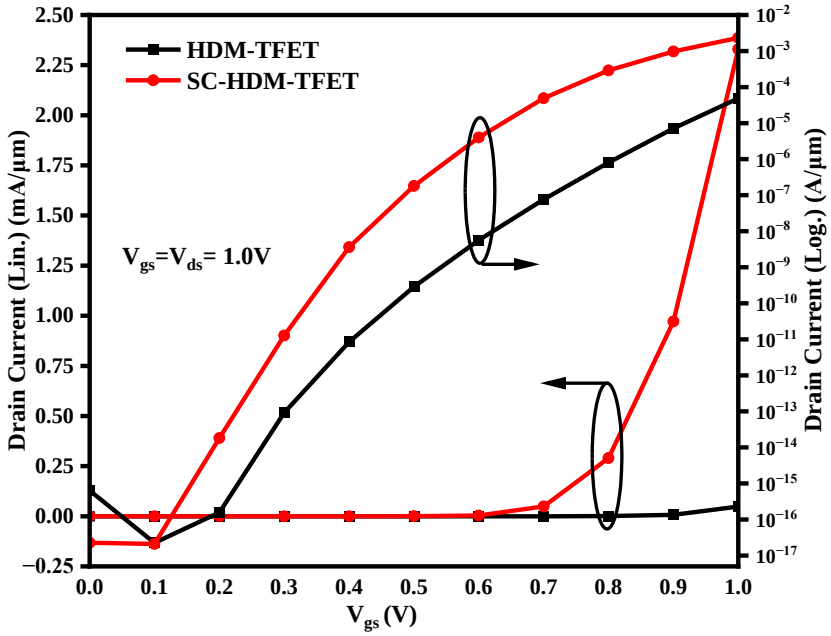

Figure 5. Illustrate the transfer characteristics of HDM-TFET & SC- HDM-TFET

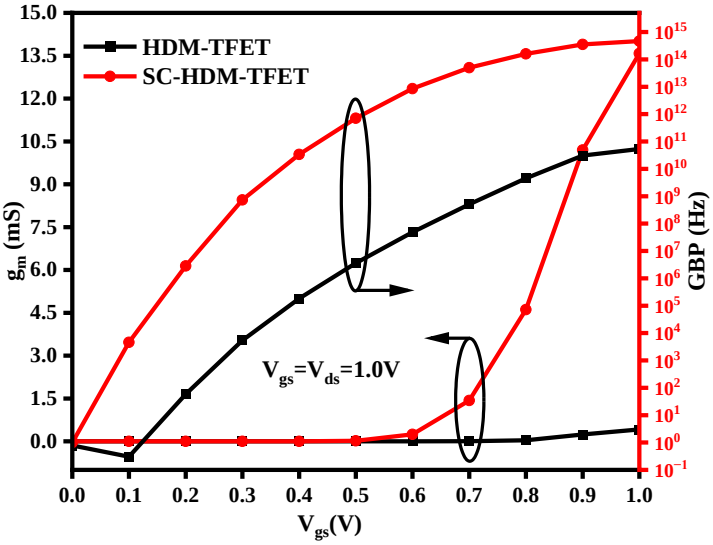

Figure 6. Shows the g_m and GBP for HDM-TFET & SC- HDM-TFET

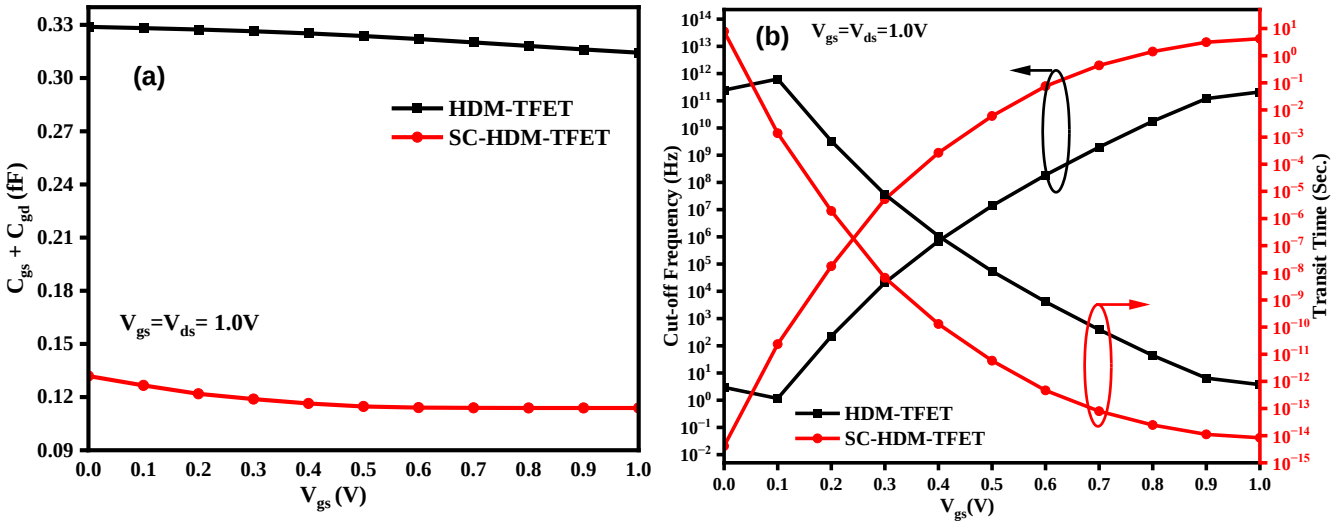

Figure 7. (a) Total capacitance **(b)** f_T and transit time w.r.t. V_{gs}

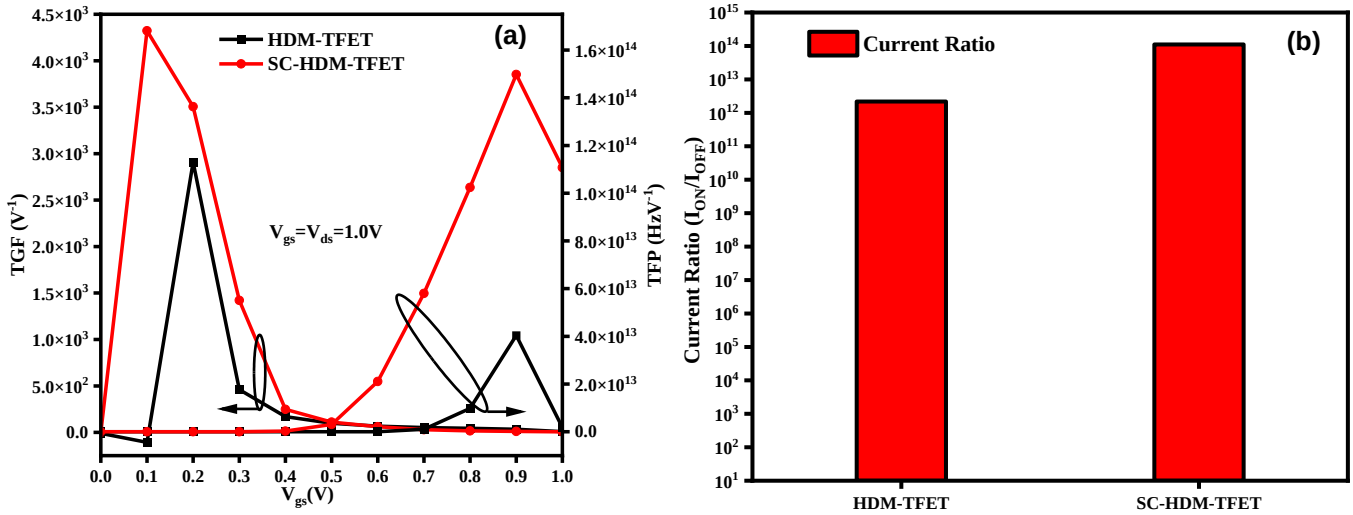

Figure 8(a). illustrates the TGF & TFP vs V_{gs} plot, **(b)** current ratio plot for both the devices

Table 2. Comparison table of DC and Analog parameters for the devices

Parameter	V_{th}	SS	g_m	I_{ON}/I_{OFF}	I_{ON}	I_{OFF}	GPB	f_T	TT
HDM-TFET	0.703	27.65	4.15×10^{-04}	$2.18\times10^{+12}$	4.87×10^{-05}	2.24×10^{-17}	$2.29\times10^{+10}$	$2.10\times10^{+11}$	7.57×10^{-13}
SC-HDM-TFET	0.454	23.77	1.36×10^{-02}	$1.11\times10^{+14}$	2.33×10^{-03}	2.27×10^{-17}	$4.69\times10^{+14}$	$1.90\times10^{+13}$	8.38×10^{-15}

3.1 DC, Analog/RF Performance and Linearity Analysis under Elevated Temperatures for Proposed Device

3.1.1 DC and Analog/RF Performance Analysis

The transfer characteristics (Id vs. Vgs) in both linear and logarithmic scales as a function of Vgs for SC-HDM-TFET is presented in figure 9(a). It is clearly demonstrated in the graph that the performance of the device has impacted with change in the temperature. The figure shows that there is a clear shift in the characteristics i.e. Ioff increases with the temperature whereas the Ion is kept almost constant. Thus the thermal stability of the device is highlighted in the figure and the device can be used for low-power, high-performance applications. For the various temperatures, gm (transconductance) and GBP (Gain-Bandwidth Product) are plotted in figure 9 (b). The plot clearly revels that both the parameters increases with increase in temperature. This suggests improved device performance at higher temperatures, which shows the thermal stability of the device along with the efficiency of SC-HDM-TFET in high-performance applications.

Cut-off frequency (f_T) and transit time (τ) are demonstrated in Figure 10(a) and are plotted against V_{gs} for various temperatures for the proposed device. With the increase in temperature f_T increases whereas transit time (τ) decreases due to enhanced carrier mobility and reduced delay, with lower temperatures offering superior performance due to reduced thermal scattering. The total Capacitance of the proposed device is plotted against the V_{gs} for different temperatures is plotted in Figure 10 (b). From the figure, it is very clear the total capacitance is shows higher values for increased temperatures. This degrades the performance of the device a bit but the deviation is comparatively very-2 low.

The TGF's peak at moderate V_{gs} due to optical carrier tunneling and the TFP's peak occurs at higher gate-to-source voltage, indicating improved device performance. Temperature's impact on both the parameters is clearly visible, lower temperatures lead to higher values due to reduced thermal scattering and improved carrier mobility. From figure 11(b), it can be examined that the device subthreshold swing is decreases with the increase in the temperature. Higher values of temperature result in increased carrier scattering and reduced barrier heights, results in the degradation of I_{off}, whereas Ion remains unchanged.

The behaviour of Ion and Ioff as a function of temperature for SC-HDM-TFET is illustrated in figure 12(a). The ON-current of the device increases with increase in temperature, the change in ON-current is 78% indicating enhanced tunneling efficiency due to increased thermal energy, whereas increase in I_{off} is 100% which is potentially due to increased leakage for temperature range of 200 K to 500 K. The impact of temperature variation on the threshold voltage is negative hence as temperature is increases V_{th} also decreases suggesting easier device turn-on at higher temperatures.

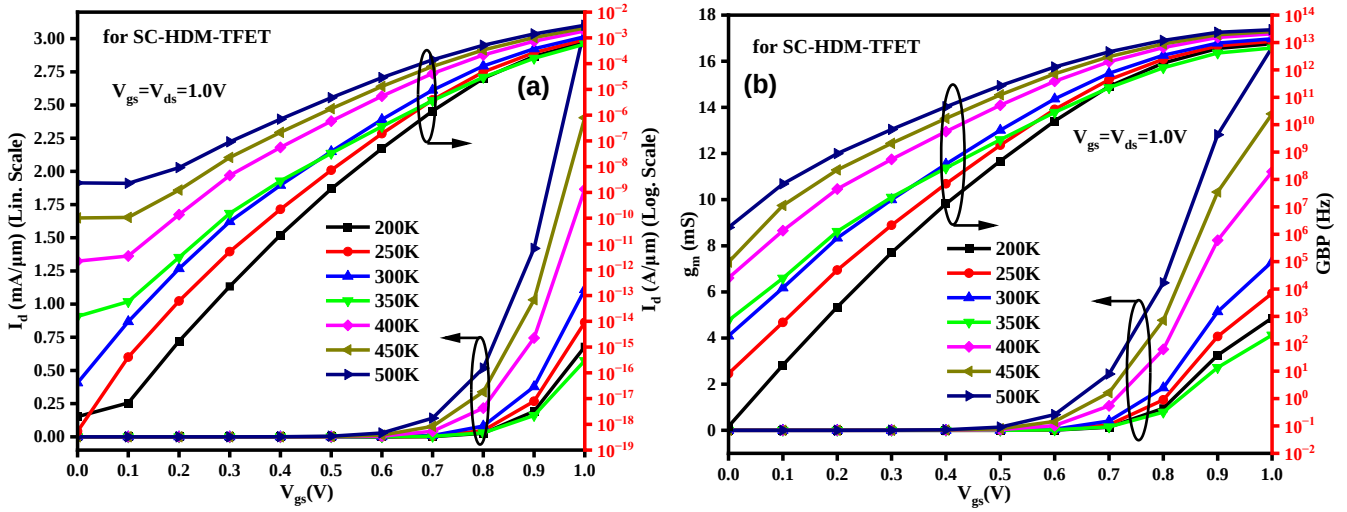

Figure 9(a). Transfer characteristic in Lin. and Log. Scale vs V_{gs} **(b)** g_m and GBP vs V_{gs} variation w.r.t. temperature

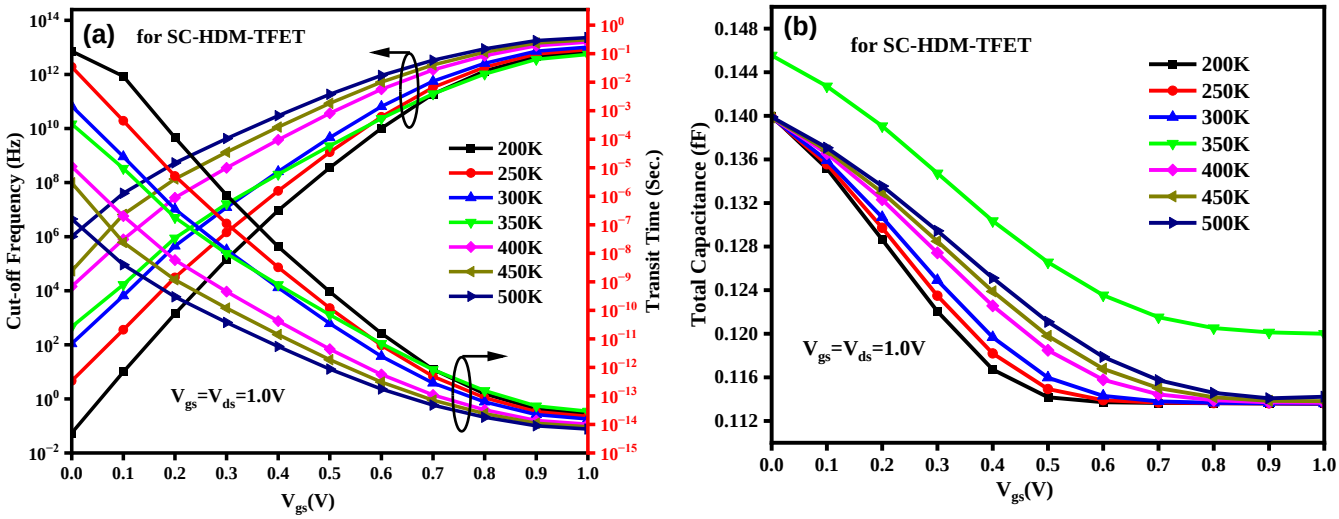

Figure 10(a). f_T and transit time vs Vgs **(b)** C_{total} vs v_{gs} variation w.r.t. temperature

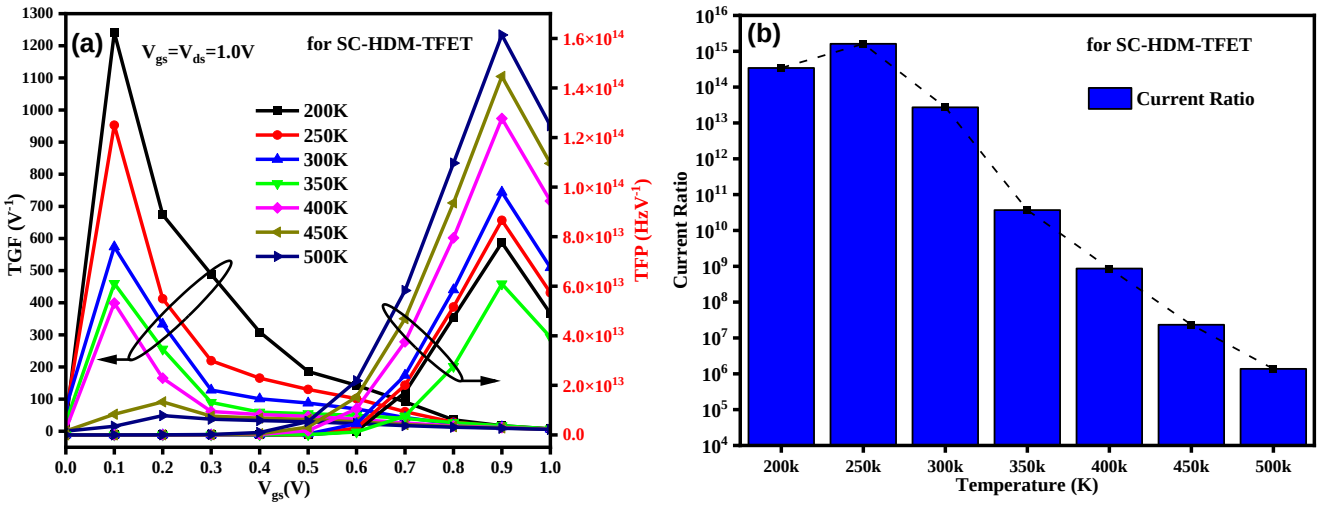

Figure 11(a). TGF & TFP vs V_{gs} **(b)** I_{on}/I_{off} vs V_{gs} variation w.r.t. temperature

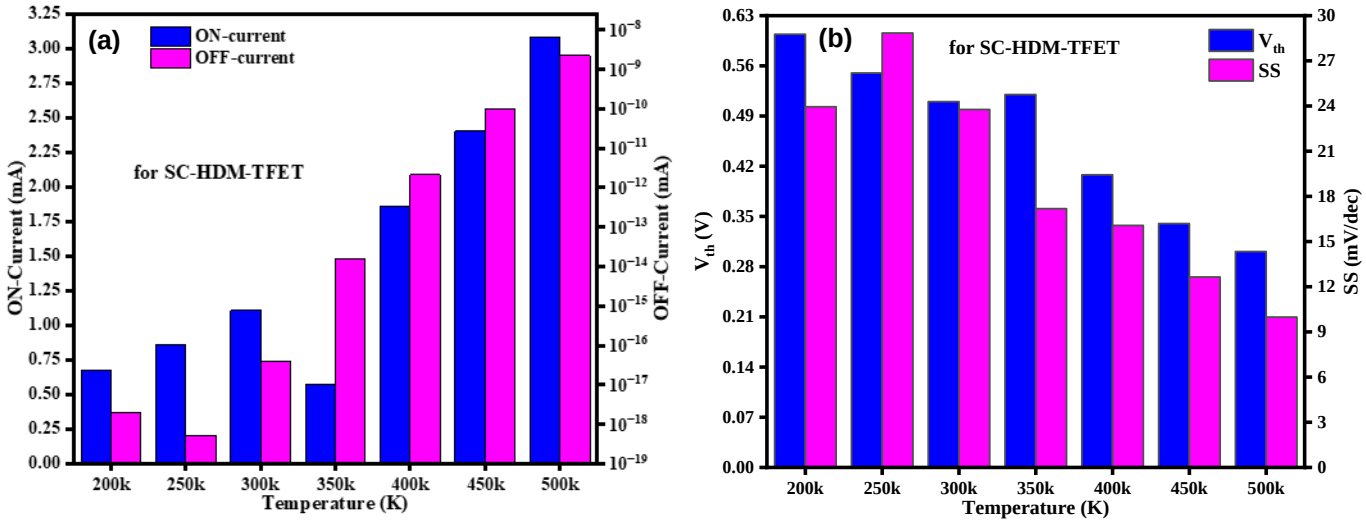

Figure 12(a). ON & OFF-current vs temperature **(b)** V_{th} and SS vs temperature

The same type of behaviour is observed for the SS indicating upgraded switching performance due to thermal effects impacting the subthreshold region. These behaviours flashes the temperature sensitivity of the proposed device, balancing performance improvements with potential leakage concerns.

3.2 Reliability Analysis

This section examines the reliability of SC-HDM-TFET across temperatures from 200 K to 500 K. We found in that thermal variations slightly increases I_{on} as temperature increases, whereas V_{th} decreases as temperature increases. However, the proposed device's subthreshold slope decreases with temperature, leading to a sharp drop in the ratio. High-frequency performance parameters also vary with temperature. Figures 13 (a) and (b) use pie charts to show the percentage deviation in DC and analog/RF characteristics. Figure 13(a) emphasizes the roles of parameters like drain current (I_d), transconductance (g_m), cutoff frequency (f_T), gain-bandwidth product (GBP), transition time (TT), and subthreshold swing (SS) in overall temperature sensitivity. In contrast, Figure 13(b) shows the sensitivity of threshold voltage (V_{th}), g_m, I_{on}/I_{off} ratio, on-state current (I_{on}), off-state current (I_{off}), transconductance gain factor (TGF), and tunneling field potential (TFP) as temperatures change. These illustrations are crucial for comprehending how temperature affects device performance, which is vital for optimizing TFET designs to ensure stable and efficient operation across various environmental conditions.

4. Linearity Analysis

This section explores the effect of temperature variation on linearity and distortion parameters.\

Second and third order transconductance (g_{m2} & g_{m3}) are plotted against gate-to-source voltage in figure 14 (a) & (b). With increase in V_{gs} and temperature higher order transconductances are increases and attain their peak value and then starts decreasing if V_{gs} is increased further. This advises that elevated temperatures make the structures more susceptible to higher-order non-linear distortions, which could negatively affect performance in applications requiring high linearity. The expressions of 2nd and 3rd-order transconductance are given in eq. 1 (a) and (b).

$$g_{m2} = \frac{\partial^2 I_d}{\partial V_{gs}^2} \quad (1a)$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial V_{gs}^3} \quad (1b)$$

Figure 15 (a) & (b) depicts the Voltage Intercept Point (2nd and 3rd order) variation w.r.t. gate-to-source voltage for different temperatures, where VIP2 shows the increasing behaviour with increasing temperature. This clearly signifies that the device is capable of handling the higher signal levels before substantial 2nd-order distortion seems, which is constructive for dipping the 2nd-order distortion. Whereas VIP3 shows reductions with higher temperatures. A lesser 3rd-order Voltage Intercept Point (VIP3) designates that the structure is more prone to third-order intermodulation distortions at elevated temperatures, which could bound its performance in high-linearity applications. The expressions of 2nd and 3rd-order Voltage Intercept Point are given in eq. 2(a) and (b).

$$VIP2 = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \quad (2a)$$

$$VIP2 = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m2}}\right)} \quad (2b)$$

Figure 16 (a) shows IIP3 versus Vgs. The input third-order intercept point (IIP3) decreases as temperature increases, suggesting the device becomes less effective at suppressing third-order intermodulation products at higher temperatures. Figure 16 (b) displays IMD3 versus Vgs, where IMD3 decreases with lower temperatures.

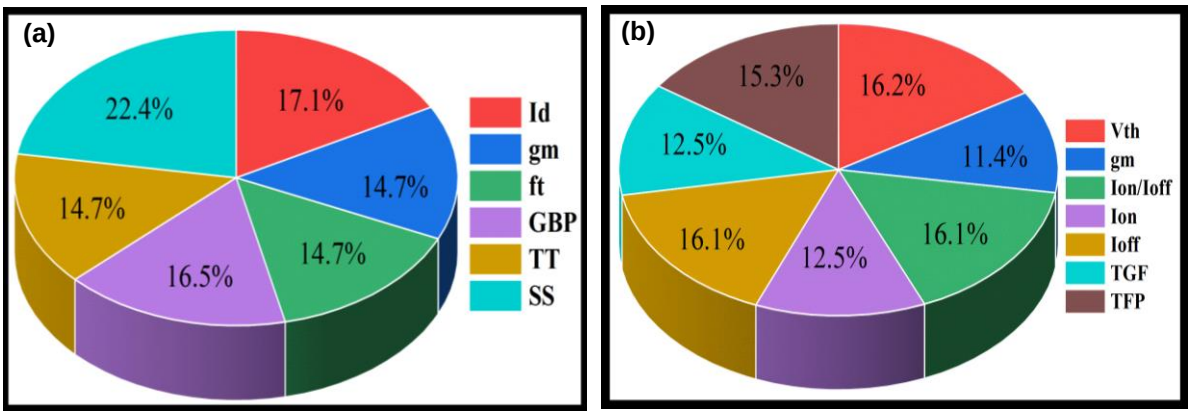

Figure 13 (a) & (b) Pi chart of temperature sensitivity for DC and Analog/RF parameters

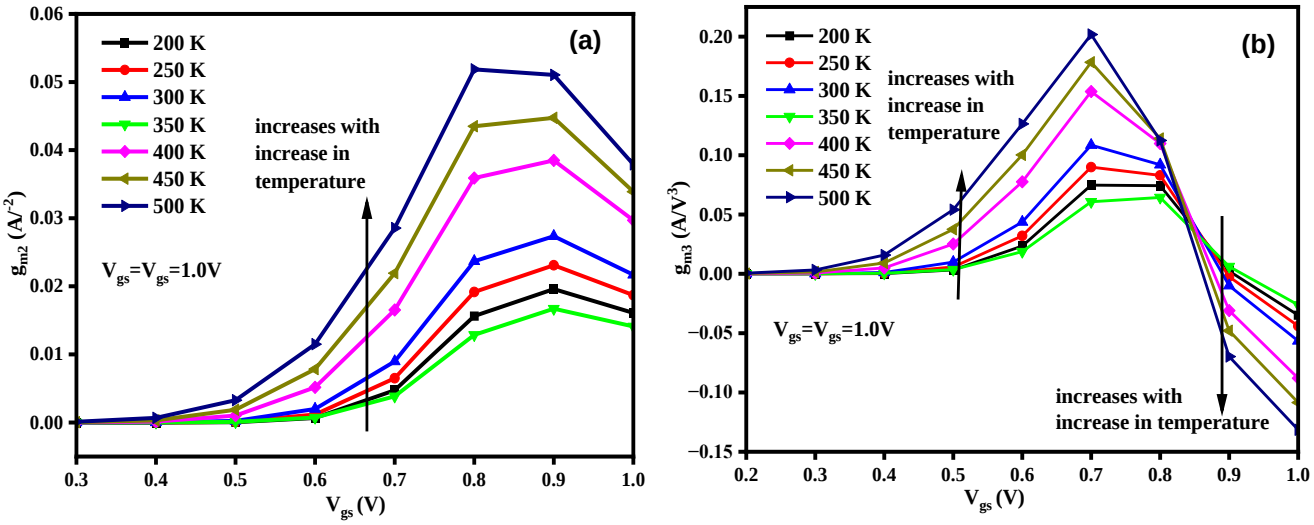

Figure 14(a). g_{m2} vs V_{gs} **(b)** g_{m3} vs V_{gs} shows the impact of temperature variation

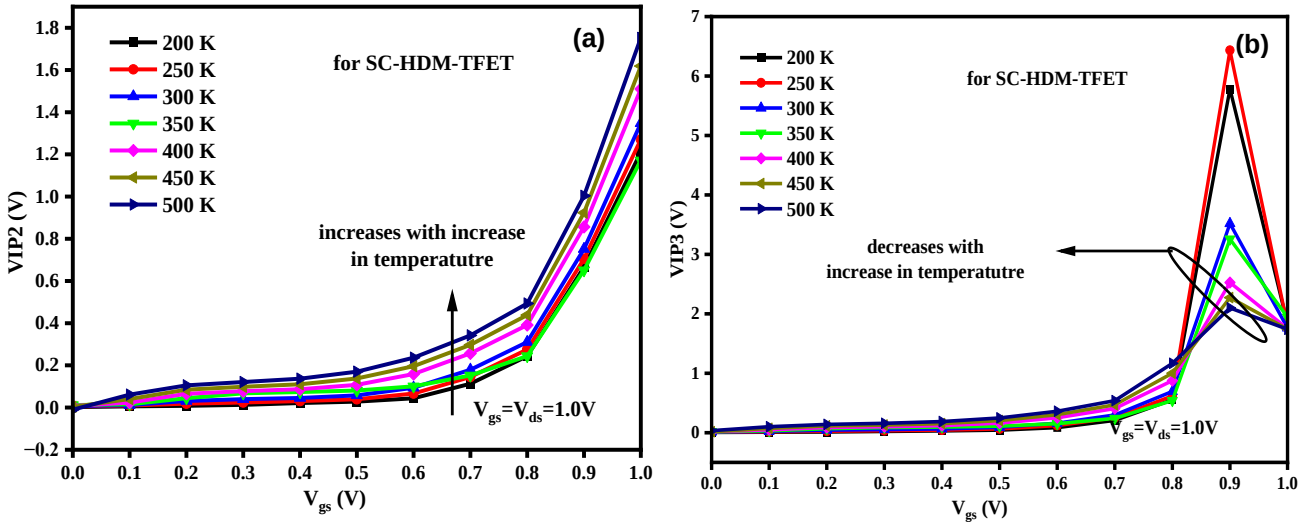

Figure 15 (a). VIP2 vs Vgs **(b)** VIP3 vs Vgs illustrate the impact of temperature variation

This indicates that reducing the operating temperature helps minimize third-order intermodulation distortions, improving overall linearity. The mathematical relations of IIP3 and TMD3 are given below in eq. 3 (a) and (b) –

$$IIP3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_S} \quad (3a)$$

$$IMD3 = \left[\frac{9}{2} \times (VIP3)^2 \times g_{m3}\right]^2 \times R_S \quad (3b)$$

Figure 17 (a) presents HD2 versus V_{gs}, showing that second harmonic distortion (HD2) decreases with increasing temperature. This behavior is somewhat unexpected given the increase in g_{m2}, suggesting complex interactions in the device's characteristics.

Figure 17 (b) illustrates HD3 versus V_{gs}, where third harmonic distortion (HD3) also decreases at higher temperatures, despite the rise in g_{m3}, pointing to compensatory mechanisms within the device. The expressions of 2nd and 3rd-order harmonic distortions are given in eq. 4(a) and (b).

$$HD2 = \frac{1}{2} V_a \frac{\frac{dg_m}{dV_{gs}}}{2g_m} \quad (4a)$$

$$HD3 = \frac{1}{2} V_a^2 \frac{\frac{d^2 g_m}{dV_{gs}^2}}{6g_m} \quad (4b)$$

Figure 18 (a) shows total harmonic distortion (THD) versus V_{gs} for 200 K to 500 K temperature range. Total harmonic distortion (THD) shows the inverse behaviour with the temperature i.e. it increases with decrease in temperature and decreases with increase in temperature, signifying a development in overall linearity with higher temperatures. Figure 18 (b) displays the 1-dB compression point (CP) w.r.t. gate-to-source voltage. The 1-dB CP has shown the direct relation with temperature, which signifies that the device can handle more and more power without significantly affecting the gain compression at elevated temperatures, which is beneficial for power amplifier applications. THD and 1-dB CP are expressed below in eq. 5 (a) & (b) –

$$THD = \sqrt{(HD2)^2 + (HD3)^2} \quad (5a)\ [44]$$

$$1\ dB = 0.22 * \sqrt{\frac{g_m}{g_{m2}}} \quad (5b)$$

The comparison of this work with the previously reported work is tabulated in table III below.

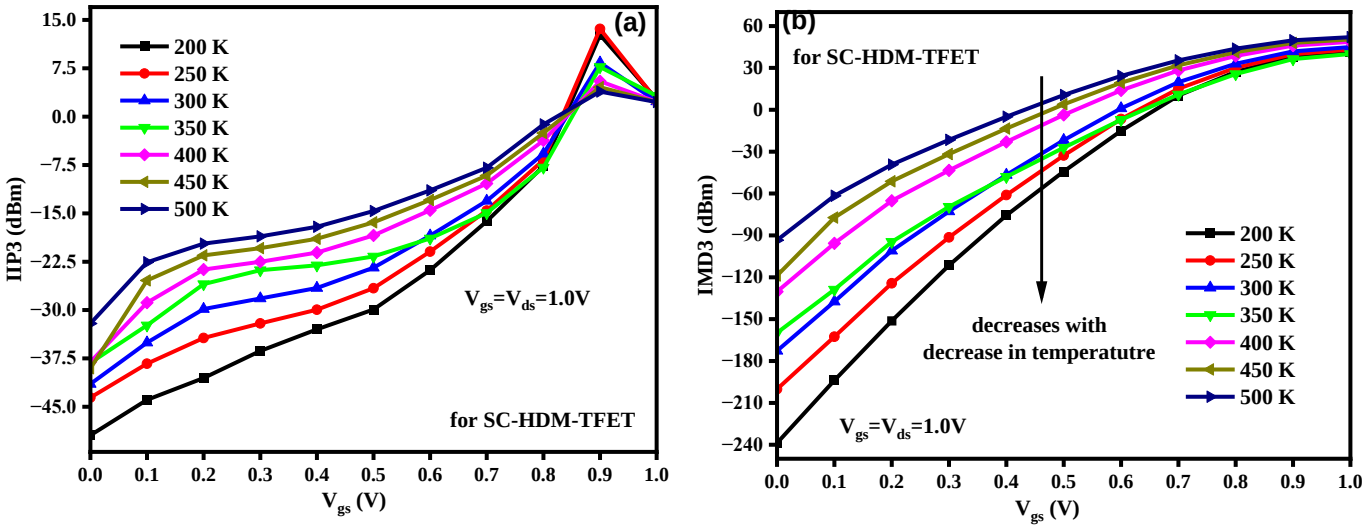

Figure 16(a). IIP3 vs V_{gs} **(b)** IMD3 vs V_{gs} illustrate the impact of temperature variation

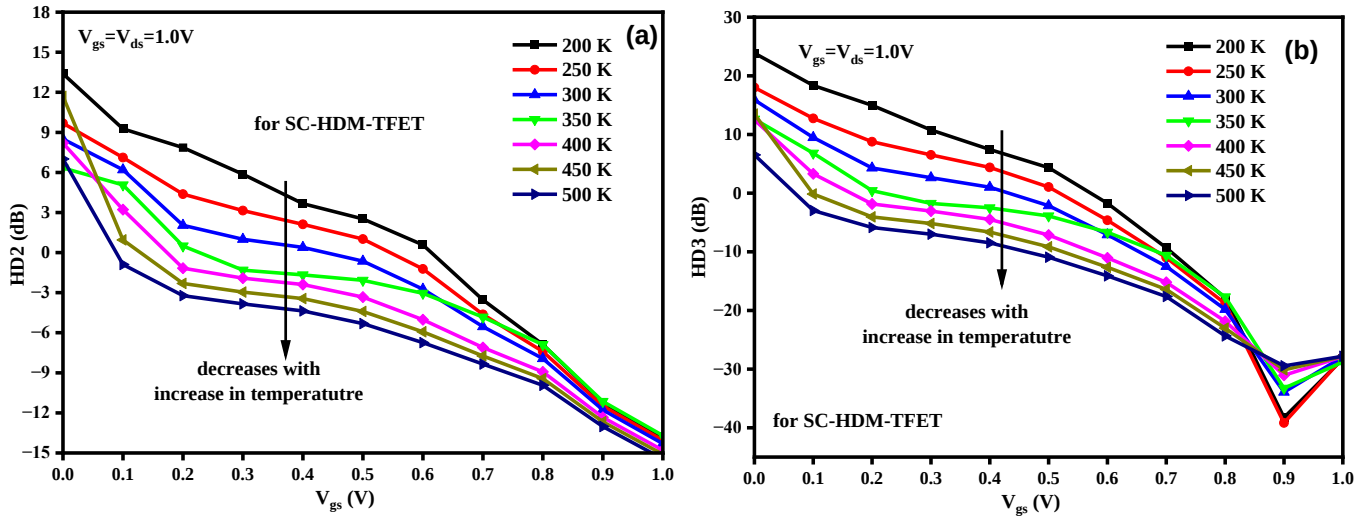

Figure 17(a). HD2 vs V_{gs} **(b)** HD3 vs V_{gs} shows the impact of temperature variation

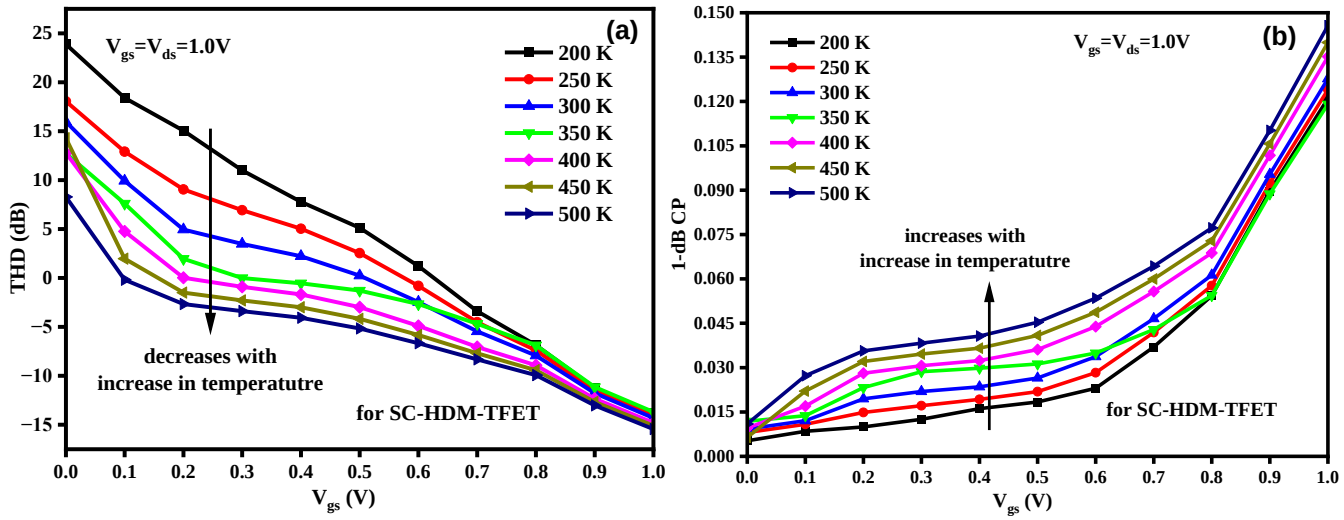

Figure 18(a). THD vs V_{gs} **(b)** 1-dB (CP) vs V_{gs} displays the impact of temperature variation

Table 3. Comparison with previous work

Parameter	SC-HDM-TFET	[52]	[53]	[54]	[55]
V_{th}	0.454	0.41	-	-	0.6
SS (mV/dec)	23.77	-	41.54	25.31	54
I_{on} (A/μm)	2.33×10^{-03}	1.21×10^{-4}	10^{-3}	-	2.40×10^{-03}
I_{off} (A/μm)	2.27×10^{-17}	1.23×10^{-13}	10^{-17}	-	-
Ratio	$1.11\times10^{+14}$	$9.83\times10^{+11}$	10^{+12}	$5.23\times10^{+11}$	$\sim10^{-14}$

5. Conclusion

In this work, we have done the comparative analysis for the DC and Analog/RF parameters between HDM-TFET and SC-HDM-TFET along with the detailed analysis of SC-HDM-TFET for DC & Analog/RF and linearity performance analysis for temperature range of 200 K – 500 K @ 50 K. SILVACO TCAD – 2D tool is used for performing the simulations. The results illustrate that the device SC-HDM-TFET has shown the enhanced stability and stability in the metrics under temperature changes, while the SC-HDM-TFET outperforms in harmonic distortion and its temperature sensitivity.

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Authors Contribution Statement
Rajeev Kumar Sachan: Conceptualization, Methodology, TCAD software, Data curation, Writing—Original draft preparation, Investigation. Vedvrat: Analysis and interpretation of data, Visualization, Validation, Writing, Review and Editing. Vidyadhar Gupta: Revision, Writing, Review and Editing. Shrish Bajpai: Supervision and Writing, Review and Editing All the authors read and approved the final version of the manuscript.

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Competing Interests
The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

Data Availability
The data supporting the findings of this study can be obtained from the corresponding author upon reasonable request.

Has this article screened for similarity?
Yes