RESEARCH ARTICLE

INTERNATIONAL RESEARCH JOURNAL OF MULTIDISCIPLINARY TECHNOVATION

Asian Research Association

DOI: 10.54392/irjmt25311

Performance Optimization of Germanium-Graphene Heterojunction Tunnel Field Effect Transistor using Dual Metal Strip

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DOI: https://doi.org/10.54392/irjmt25311

Received: 21-02-2025; Revised: 19-04-2025; Accepted: 22-04-2025; Published: 04-05-2025

Abstract: This work presents and investigates a Dual Metal Gate Graphene Nanoribbon (DMHGNR) with a Germanium heterojunction-based Tunnel Field-Effect Transistor (DMHGNRTFET). The impact of a dual metal strip combined with a hetero-dielectric on the heterojunction TFET architecture is analyzed. Optimization of the ON/OFF current and their ratio is achieved by the use of design engineering, bandgap engineering, and work function engineering. Simulations are carried out to evaluate the proposed DMHGNRTFET together with GNRGeTFET and GNRSiTFET by examining surface potential, energy band diagrams, carrier concentration, electric field distribution, I_d-V_{gs} characteristics, and transconductance. The DMHGNRTFET exhibits an I_{on}/I_{off} ratio of approximately 10^{12}, alongside a minimal subthreshold swing (SS) of 33.9 mV/decade. It features the lowest threshold voltage observed at 0.41 V and achieves a maximum I_{on} of 2.44×10^{-4} A/μm. The findings of SILVACO TCAD simulations suggest the potential for enhanced performance in low power applications of the DMHGNRTFET.

Keywords: Graphene, Hetero Structure, Dual Metal Strip, Hetero Dielectric, Current Ratio

1. Introduction

Moore's Law drives continuous miniaturisation of CMOS technology by predicting the raising integration of transistor count in an integrated circuit (IC) [1]. Smaller, more efficient, and high-performance devices follow from this accelerating speed of computer development. Transistors shrink as technology advances and packing density rises—a phenomena often referred to as scaling [2]. Among the various benefits of scaling are more rapid switching rates, smaller chip sizes, and reduced power consumption. On the other hand, there are disadvantages to consider, such as short-channel effects (SCEs), which have an adverse influence on device performance as the channel length reduces [3]. One may choose from several scaling strategies, such as constant voltage scaling or full scaling. Full scaling involves reducing all device parameters by a value 's', while constant voltage scaling keeps the voltage constant. Short-channel effects (SCEs) and leakage currents have grown to be main problems in CMOS technology as technological nodes develop [4]. Performance deteriorates in part from factors like Drain-Induced Barrier Lowering (DIBL), sub-threshold slope (SS), and the hot electron effect [5]. Similarly, the SS threshold limit sets limitations on conventional MOSFETs [6].

Tunnel field effect transistors (TFETs) have emerged as a viable substitute to deal with these issues. TFETs use a PIN junction and depend on Band-to- Band Tunnelling (BTBT) for conduction unlike MOSFETs. These are a potential option for power efficient applications because to their unique working mechanism, which allows them to transcend the SS limit of 60 mV/dec [7-9]. Two primary issues associated with TFET devices, notwithstanding their advantages, are ambipolarity and reduced ON-state current (I_{on}) in comparison to CMOS technology. The presence of low I_{on} current results in a decrease in switching speed. Multiple approaches have been explored to enhance I_{on}, including gate architecture engineering, gate oxide engineering, heterojunction engineering, strained bandgap engineering, and electrostatic control engineering [10–22]. Among these options, multi-gate engineering has demonstrated the highest level of success.

The TFET with dual gates (DGTFET) architecture is introduced to improve the electrical performance [23, 24]. The additional gate provides superior control over leakage current, rendering it highly suitable for low-power applications and standby devices. Germanium serves as a viable alternative to silicon due to its lower energy bandgap and enhanced carrier mobility. Recent research investigates nano-transistors

to enhance device performance through the utilization of nanotubes or nanowires. Graphene, particularly graphene nanoribbons (GNRs), has received attention for low-power applications due to its adjustable bandgap and high carrier mobility, thereby improving ON-current in TFETs [25, 26]. In addition to conventional silicon channels, graphene nanoribbons (GNRs) offer a feasible bandgap that facilitates effective band narrowing (BTBT) and enhances carrier transportation [27]. Their unique electrical, mechanical, and thermal properties, influenced by width and edge configurations (armchair or zigzag), render them essential for advancements in nanotechnology and electronics. Additionally, research demonstrates that the Low Work Function Strip (LWS) methodology [28] enhances the performance of plasma-based TFETs. The DG-TFET with LWS alone does not yield the anticipated ion enhancement. An enhanced method utilising single metal strips within the oxide region adjacent to the source-channel junction is reported to further enhance performance, as indicated in reference [29].

No research has been conducted to investigate the utilisation of double metal segments in DG-TFETs at yet. The present work introduces and examines a novel device architecture: the Dual Metal Hetero GNR based Tunnel Field-Effect Transistor (DMHGNRTFET). A comparison study is conducted among DMHGNRTFET, Single Metal GNR-Ge sourced TFET (GNRGeTFET) and Single Metal GNR-Si sourced TFET (GNRSiTFET), and based on Analog/RF criteria to evaluate their performance. The following describes the organization of this work: Section 1 offers a review. Section 2 addresses the device architecture and simulation setting. Section 3 shows the simulation results. Section 4 offers a synopsis of the conclusions reached.

2. Device Description and Simulation Methodology

The Double Gate configuration enhances ON-state current (I_{on}) and optimizes electrostatic control at the gate terminal. Figure 1(a-c) shows the sectional view of the outlined DMHGNRTFET, GNRGeTFET, and GNRSiTFET architecture respectively. The device has a 30 nm gate length and a 10 nm silicon body thickness (T_{Si}), achieved by body thickness optimization. The Nickel (Ni) metal strips utilized in the simulation exhibit a work function of 4.9eV, while the gate metal work function ($\emptyset_m$) is established at 4.0 eV. All physical dimensions and design specifications are consistently upheld across the examined configurations, ensuring an equitable assessment of device performance. Table 1 provides a comprehensive summary of the structural elements and material properties utilized in the simulation. Table 1 shows that an added pair of metal strips (DM), each having a length of 10 nm and a thickness of 0.5 nm, is found integrated at the source/drain-channel junctions inside the oxide layer. The dual metal strip structure in DM-DGTFET is formed with these strips being electrically connected to the gate electrode. Simulations conducted using the Silvaco TCAD tool [30]. Tunneling currents, highly reliant on junction band bending and semiconductor characteristics, are accounted for using a non-local tunneling model [31]. To precisely depict large source doping concentrations, also a band-gap narrowing model is used. Multiple complex simulation models accurately describe challenging physical phenomena for device characterization. These include Fermi-Dirac statistics, which show carrier dispersion more realistically, particularly at high doping concentrations, and field-dependent mobility models, which explain carrier mobility variations under different electric fields.

Table 1. Device Parameters for Designed Distinct Device Structures

Specification	DMHGNRTFET	GNRGeTFET	GNRSiTFET
GNR Doping	1×10^{15} /cm^3	1×10^{15} /cm^3	1×10^{15} /cm^3
Si/Ge Source Doping	1×10^{20} /cm^3	1×10^{20} /cm^3	1×10^{20} /cm^3
Drain Doping	1×10^{18} /cm^3	1×10^{18} /cm^3	1×10^{18} /cm^3
Si Thickness	10 nm	10 nm	10 nm
Channel Length	50 nm	50 nm	50 nm
Source/Drain Length	30 nm	30 nm	30 nm
SiO_2/HfO_2 thickness	2 nm	2 nm	2 nm
Gate/Drain Voltage	1V/1V	1V/1V	1V/1V
Gate work function	4.0 eV	4.0 eV	4.0 eV
Metal strip Length	10 nm	-	-
Metal strip Thickness	0.6 nm	-	-
Metal strip work function	4.9 eV	-	-

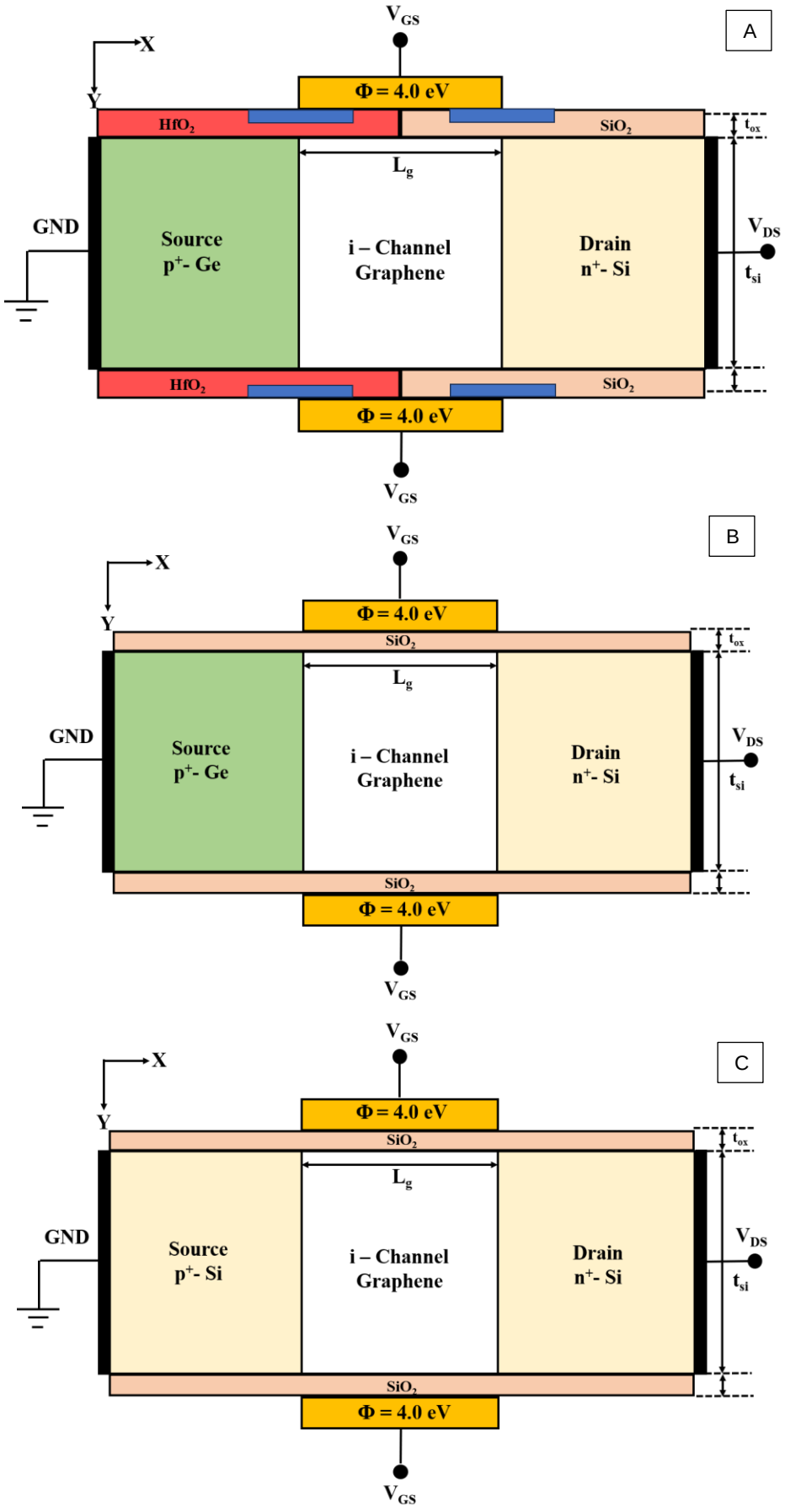

Figure 1. Schematics of (a) DMHGNRTFET, (b) GNRGeTFET, and (c) GNRSiTFET

Carrier concentration models determine charge carrier densities across the device, ensuring accurate transport predictions. The Shockley-Read-Hall (SRH) recombination model explains carrier recombination [32].

3. Results and Discussion

This subsection presents a detailed analysis and comparison of the electrical simulation results for various TFET designs, as illustrated in Figure 1. The enhancement of device performance is significantly influenced by the integration of the metal strip within the device architecture, which is accomplished through the connection of the gate electrode. The incorporation of metal strips at oxide interface facilitates to produce the sharp and steep tunneling junctions, thereby enhancing tunneling generation rate [33]. The proposed DMHGNRTFET offers more steepness at the channel-source junction by use of a metal strip with an optimized work function. Particularly, it is seen that the two metals in the stack have a substantially distinct effective work function [34]. This method allows exact control over important device parameters, hence enhancing the performance characteristics of TFETs. It particularly enables precise manipulation of the threshold voltage, which is essential to minimize off-state leakage currents and achieve optimal switching behavior. Furthermore, this approach enables exact customization of the metal stack's effective work function, which is important in determining the electrostatic control over the channel. As illustrated in Fig. 3, a steeper tunneling junction results from an energy band valley created by the metal strip [35]. The conduction and valence bands are pushed down when V_{gs}= V_{ds}= 1V, hence lowering the BTBT barrier at the channel-source contact. By improving band alignment between the source and channel regions, the inclusion of the metal strip essentially reduces the tunneling barrier, hence boosting subthreshold swing (SS) and raising Ion at lower gate voltages (V_{gs}).

Figure 2 illustrates the transfer characteristics (I_d-V_g) of the various TFET designs examined in this study. Devices with identical physical dimensions and doping concentrations were evaluated to highlight the advantages of the metal strip approach. The results indicate that the elevated electric field associated with the metal strip approach significantly enhances drain current performance. The DMHGNRTFET configuration demonstrates superior performance compared to both GNRGeTFET and GNRSiTFET among the examined configurations. Replacing the oxide area with a metal strip results in the closure of the channel region's gap, thereby leading to an increase in the gate's leakage current (I_{off}) in DMHGNRTFET, as illustrated in Figure 2.

Illustrated in Figure 3, the energy diagram of the suggested structure demonstrates explicit conduction and valence band alignments in different operational states. A small energy step in the band structure may be seen from the heterojunction presence. Through change of the potential energy profile, this heterojunction-induced step affects carrier dynamics. The energy gap between the conduction and valence bands at the source-channel contact is much reduced in the ON state. This reduction of the band separation promotes quantum tunnelling, therefore allowing charge carriers to pass the barrier more quickly. As such, the operational efficiency of the device depends much on this tunnelling effect, which improves its switching performance and general electrical properties.

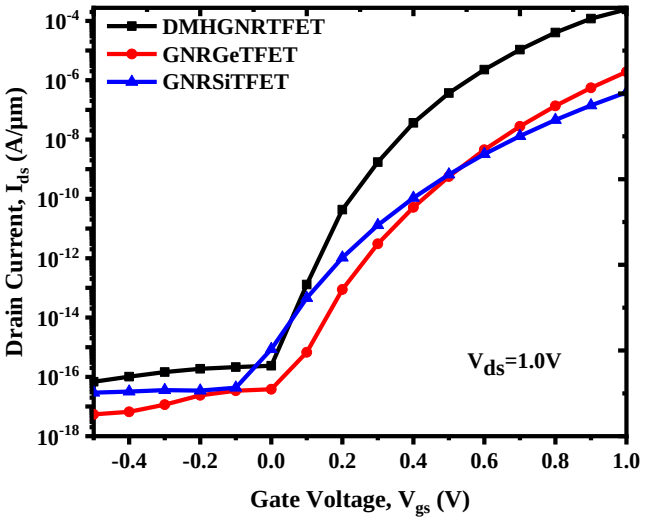

Figure 2. I_d-V_{gs} characteristics comparison of DMHGNRTFET, GNRGeTFET and GNRSiTFET

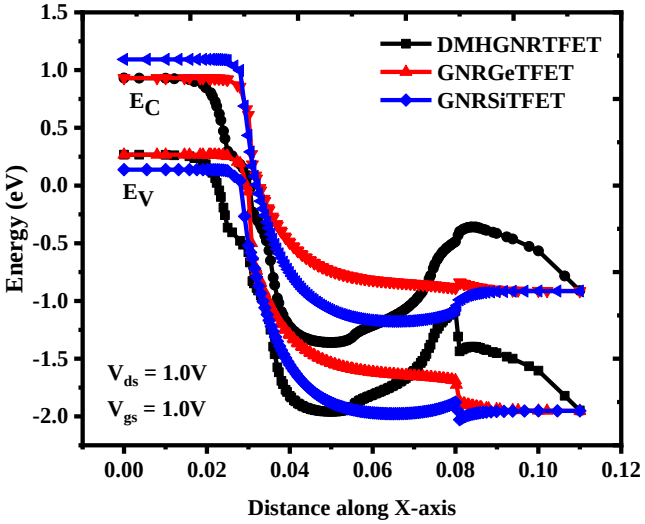

Figure 3. Energy band diagram variation of DMHGNRTFET, GNRGeTFET and GNRSiTFET along lateral distance in ON state

The hole concentration distribution inside the DMHGNRTFET device is shown in figure 5; the concentration at the source is greater than that at the drain proximity. Minimal volatility of the channel area suggests steady charge carrier behaviour over its length. Among the main structural features of the DMHGNRTFET, the PIN design shows the most notable change in electron/hole concentration from the source to the drain.

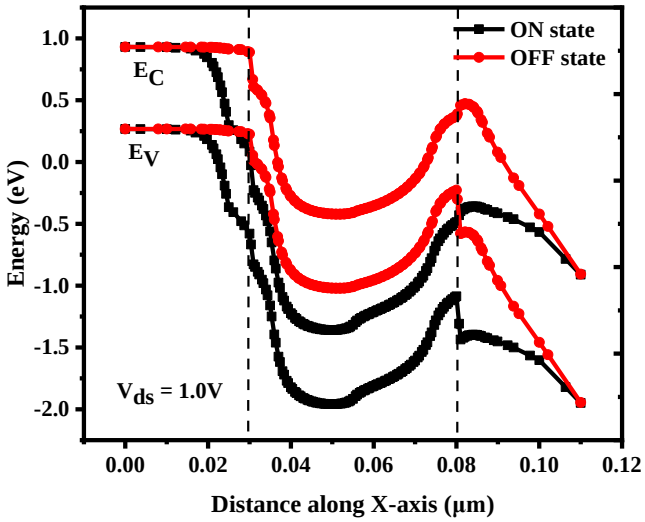

Figure 4. Energy band diagram of DMHGNRTFET in ON state and OFF state

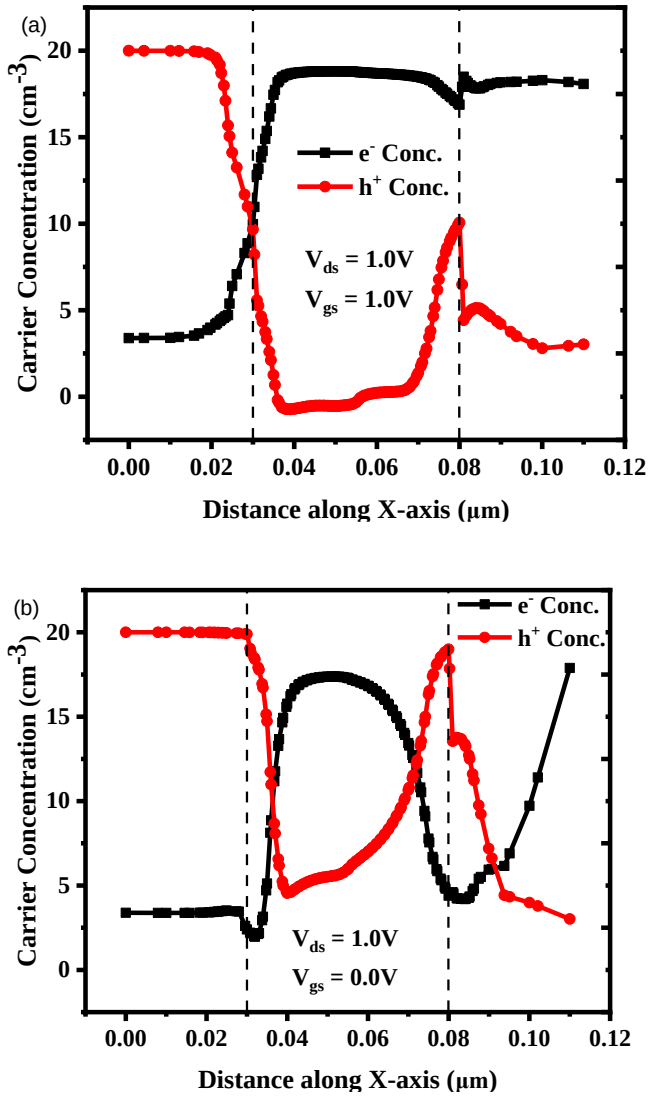

Figure 5. Carrier concentration variation in DMHGNRTFET with lateral distance in (a) ON state and (b) OFF state

The red-coloured line in Figure 5(a) emphasises the greatest hole concentration happening at the source area in the operating state, which progressively reduces towards the drain. Furthermore, the graphic offers understanding of the fluctuation in electron concentration along the channel length. A key transition point for carrier injection is indicated by a rapid shift in electron concentration seen at the source-channel interface in the ON state. Outside of this interface, the channel area experiences relatively little variations. Moreover, the current (I_d) depends much on the availability of free electrons. Variations in electron concentration throughout the device length alter the charge transport kinetics, therefore influencing the drain-side properties. The general efficiency and performance of the device are controlled by the interaction of electron concentration with drain driving current. Figure 5(b) shows the carrier concentration variation in OFF state along the device lateral length.

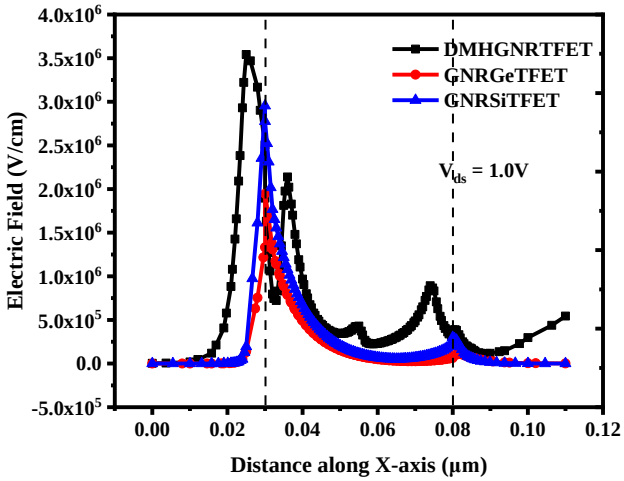

Figure 6. Electric field variation in DMHGNRTFET, GNRGeTFET and GNRSiTFET along lateral distance in ON state

Electric field fluctuations over device channel length are shown in Figure 6 for three distinct configurations of the proposed device designs. The investigation highlights the variation in electric field distribution across different configurations, thereby providing insights into the impact of structural and material modifications on the electrostatic behaviour of the device. The final design of the DMHGNRTFET, which integrates a germanium (Ge) and graphene nanoribbon (GNR) heterojunction with a dual metal layer, exhibits the most pronounced electric field fluctuation at the source-channel interface among the three configurations. The integration of these elements enhances the electric field intensity at the contact point, which is crucial for facilitating efficient charge carrier transfer and tunnelling processes. The results demonstrate the impact of material engineering and multi-layered metal gate construction on the general device performance. The final configuration of the DMHGNRTFET demonstrates improved carrier injection

efficiency through the optimisation of the electric field distribution.

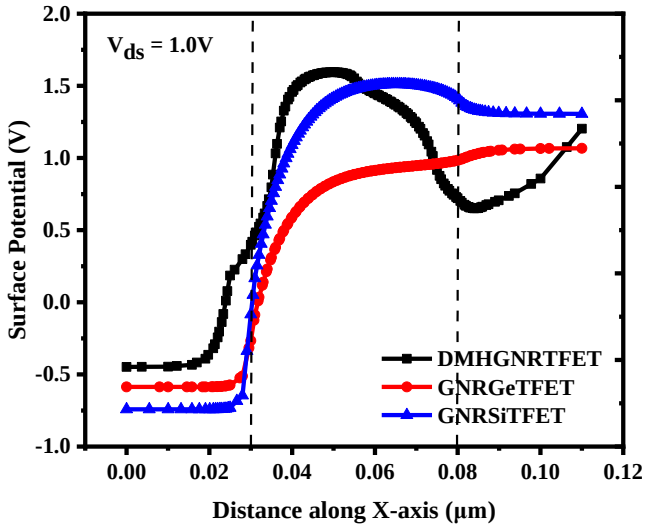

Figure 7. Surface Potential variation in DMHGNRTFET, GNRGeTFET and GNRSiTFET along lateral distance

Figure 7 illustrates the variations in surface potential across the three device configurations. The figure indicates that in the most recent proposed configuration, both the surface potential and the electric field increase simultaneously across the tunnelling region extending from the source to the channel. This enhancement is more distinctly evident compared to the other two combinations. The observed increase in surface potential can be primarily attributed to the integration of a twin metal layer and the PIN configuration within the heterostructure TFET. The use of a low-bandgap compound material at the source-channel junction further facilitates effective carrier transport, thereby enhancing tunnelling properties. However, due to the complexity of the doping insertion technique, this PIN configuration may lead to higher manufacturing costs, despite the potential enhancement in device performance.

Figure 8 illustrates the differences in transconductance among the three device designs. The DMHGNRTFET structure demonstrates optimal transconductance values as indicated by the transconductance curve, thereby confirming its superior efficiency in converting an applied voltage into proportional current amplification. The GNRSiTFET arrangement demonstrates suboptimal performance in current amplification, exhibiting the lowest conversion efficiency in response to variations in the applied gate voltage.

Figure 9 presents a statistical analysis of (a) threshold voltage and subthreshold swing, (b) ON-OFF current, and (c) I_{ON}/I_{OFF} ratio, highlighting four primary performance variances among the proposed device designs. The distinct value of each parameter facilitates a direct comparison of device performance. Among the three designs evaluated, the PIN DMHGNRTFET exhibits superior performance metrics. Fig. 9(a) demonstrates the capability of the DMHGNRTFET structure to attain the lowest threshold voltage and subthreshold swing, highlighting its enhanced switching performance. Fig. 9(b) illustrates enhanced efficiency, demonstrating a maximum ON-state current of 2.44×10^{-4} A/µm and a minimum OFF-state current of 6.80×10^{-17} A/µm, thereby ensuring reduced leakage and improved power economy.

Fig. 9(c) illustrates the I_{on}/I_{off} current ratios for the three designs, providing a comparative analysis. The I_{on}/I_{off} values for DMHGNRTFET, GNRGeTFET, and GNRSiTFET are 3.59×10^{12}, 3.50×10^{11}, and 1.32×10^{10}, respectively. Of the evaluated designs, the DMHGNRTFET demonstrates the highest efficiency, evidenced by the superior I_{on}/I_{off} current ratio and a minimal subthreshold swing (SS) of 33.95 mV/decade.

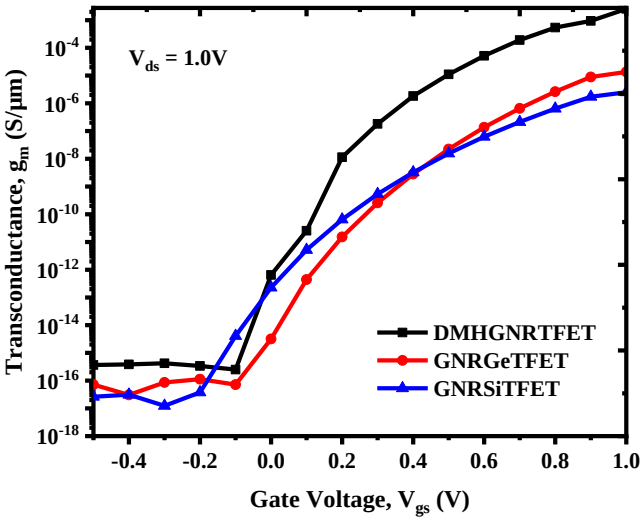

Figure 8. Transconductance variation in DMHGNRTFET, GNRGeTFET and GNRSiTFET with gate voltage

Table 2. Performance Comparison of Designed Distinct Device Structures

FoMs	DMHGNRTFET	GNRGeTFET	GNRSiTFET
I_{on}/I_{off}	3.59×10^{12}	3.50×10^{11}	1.32×10^{10}
I_{on} (A/µm)	2.4×10^{-4}	1.9×10^{-6}	3.9×10^{-7}
V_{th} (V)	0.41	0.76	0.85
SS (mv/decade)	33	47	58

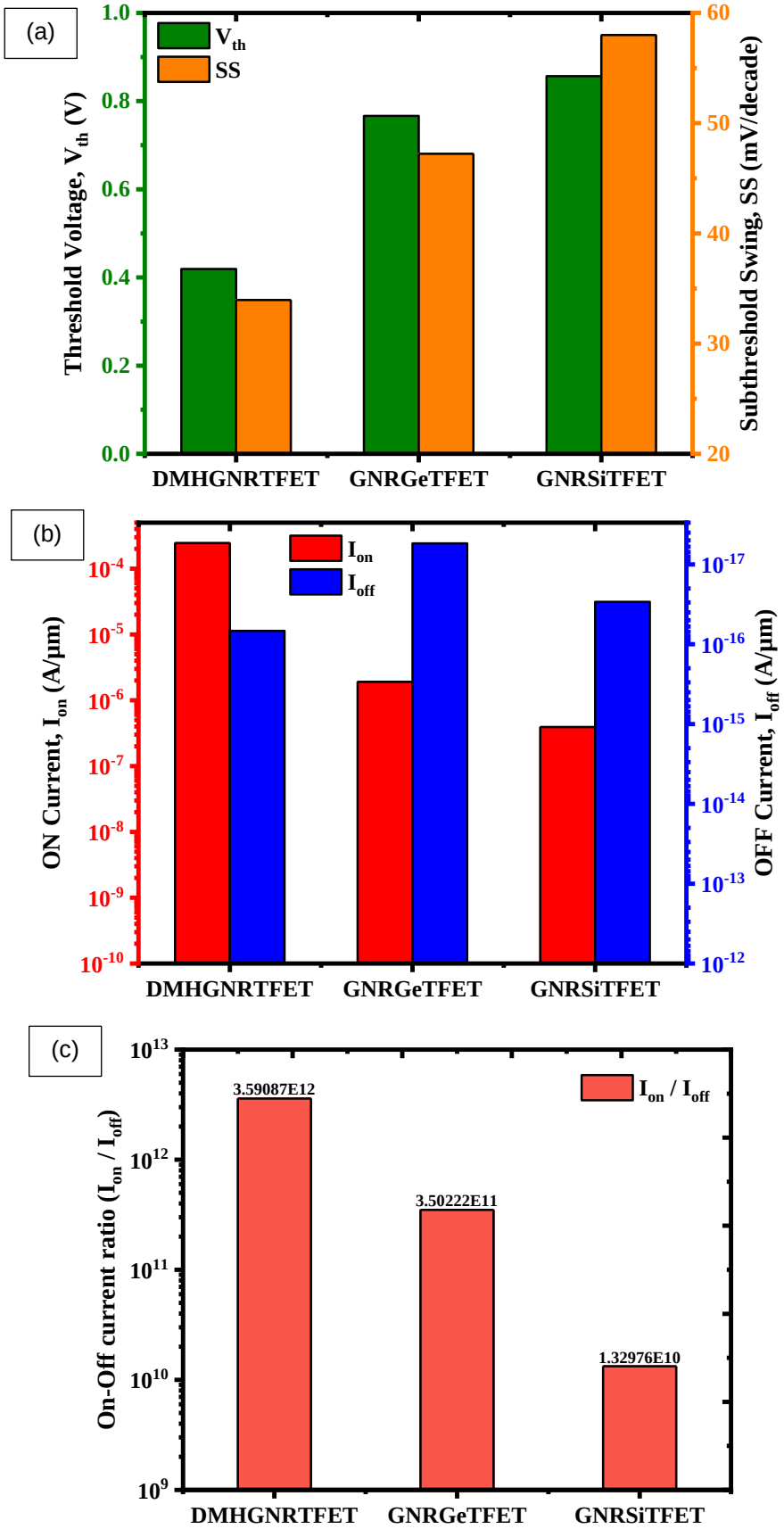

Figure 9. Comparison of (a) ON current and OFF current, (b) threshold voltage and subthreshold swing for designed device structures

A higher subthreshold slope, in conjunction with a favourable average subthreshold slope (AVSS), facilitates rapid switching with minimal latency. The recorded AVSS values for DMHGNRTFET, GNRGeTFET, and GNRSiTFET are 33.95 mV/dec, 47.22 mV/dec, and 58 mV/dec, respectively. The

comparative study of the designed structures is shown in Table. 2. The results indicate that the DMHGNRTFET structure is the most promising candidate among the proposed designs, as it demonstrates superior performance regarding threshold voltage, switching efficiency, and current control.

5. Conclusion

This work investigates a new Dual Metal heterojunction GNR based TFET (DMHGNRTFET) utilizing the Silvaco TCAD tool. The evaluation focuses on its electrical properties, which include the energy band diagram, electron and hole carrier concentration, electric field distribution, transfer characteristics (Id–Vgs), surface potential, and transconductance. Integrating metal strips into the device structure enhances the internal electric field, resulting in superior performance compared to Ge sourced Graphene nanoribbon TFET (GNRGeTFET) and Si sourced Graphene nanoribbon TFET (GNRSiTFET). Hot carrier injection results in an increase in gate leakage current. The integration of metal strips leads to an enhancement in internal voltage amplification, significantly boosting the ON current (Ion) and reducing the subthreshold slope (SS). Three TFET architectures, DMHGNRTFET, GNRGeTFET, and GNRSiTFET, are developed, contrasted, and examined based on their electrical performance. DMHGNRTFET exhibits the Ioff value of $6.80 \times 10^{-}17$ A/μm and the highest Ion value of $2.44 \times 10^{-}4$ A/μm. The incorporation of metal strips results in an impressive Ion/Ioff ratio of nearly 1012 order. Furthermore, of all the configurations examined, DMHGNRTFET exhibits the lowest subthreshold slope of 33.95 mV/decade, indicating its suitability for applications requiring low-delay and high-speed switching. DMHGNRTFET exhibits significant potential for application in advanced circuits and systems, where energy efficiency and rapid switching speed are critical factors, due to its enhanced performance characteristics.

References

[1] M.M. Waldrop, The chips are down for Moore's law, Nature News, 530(7589), (2016) 144. https://doi.org/10.1038/530144a

[2] B. Hoefflinger, IRDS—International Roadmap for Devices and Systems, Rebooting Computing, S3S, in NANO-CHIPS 2030: On-Chip AI for an Efficient Data-Driven World, (2020) 9–17. https://doi.org/10.1007/978-3-030-18338-7_2

[3] S. Veeraraghavan, J.G. Fossum, Short-channel effects in SOI MOSFETs, IEEE Transactions on Electron Devices, 36(3), (1989) 522–528. https://doi.org/10.1109/16.19963

[4] G.H. Jessen, R.C. Fitch, J.K. Gillespie, G. Via, A. Crespo, D. Langley, D.J. Denninghoff, M. Trejo, E. R. Heller, Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices, IEEE Transactions on Electron Devices, 54(10), (2007) 2589–2597. https://doi.org/10.1109/TED.2007.904476

[5] T.A. Fjeldly, M. Shur, Threshold voltage modeling and the subthreshold regime of operation of short-channel MOSFETs, IEEE Transactions on Electron Devices, 40(1), (1993)137–145. https://doi.org/10.1109/16.249436

[6] S.W. Sun, P.G. Tsui, Limitation of CMOS supply-voltage scaling by MOSFET threshold-voltage variation, IEEE Journal of Solid-State Circuits, 30(8), (1995) 947–949. https://doi.org/10.1109/4.400439

[7] M. Shrivastava, Drain extended tunnel FET—A novel power transistor for RF and switching applications, IEEE Transactions on Electron Devices, 64(2), (2016) 481–487. https://doi.org/10.1109/TED.2016.2636920

[8] Q. Huang, R. Huang, Z. Zhan, Y. Qiu, W. Jiang, C. Wu, Y. Wang, (2012) A novel Si tunnel FET with 36mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration, in Proc. 2012 International Electron Devices Meeting, Francisco, CA, USA, 8–5. https://doi.org/10.1109/IEDM.2012.6479005

[9] S.W. Kim, J.H. Kim, T. J. K. Liu, W.Y. Choi, B.G. Park, Demonstration of L-shaped tunnel field-effect transistors, IEEE Transactions on Electron Devices, 63(4), (2015) 1774–1778. https://doi.org/10.1109/TED.2015.2472496

[10] W.Y. Choi, W. Lee, Hetero-gate-dielectric tunneling field-effect transistors, IEEE Transactions on Electron Devices, 57(9), (2010) 2317–2319. https://doi.org/10.1109/TED.2010.2052167

[11] A.M. Ionescu, H. Riel, Tunnel field-effect transistors as energy-efficient electronic switches, Nature, 479(7373), (2011) 329–337. https://doi.org/10.1038/nature10679

[12] U.E. Avci, D.H. Morris, I.A. Young, Tunnel field-effect transistors: Prospects and challenges, IEEE Journal of the Electron Devices Society, 3(3), (2015) 88–95. https://doi.org/10.1109/JEDS.2015.2390591

[13] B.R. Raad, K. Nigam, D. Sharma, P.N. Kondekar, Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement, Superlattices and Microstructures, 94, (2016) 138–146. https://doi.org/10.1016/j.spmi.2016.04.016

[14] S. Sahoo, S. Dash, S. R. Routray, G. P. Mishra, Impact of drain doping engineering on ambipolar and high-frequency performance of ZHP line-TFET, Semiconductor Science and Technology, 35(6), (2020) 065003. https://doi.org/10.1088/1361-6641/ab7ce7

[15] S.A. Ahmad, N. Alam, Design of a triple pocket multi-gate material TFET structure for low-power applications, Semiconductor Science and Technology, 36(2), (2021) 025015. https://doi.org/10.1088/1361-6641/abcdf9

[16] K.K. Kavi, S. Tripathi, R. A. Mishra, S. Kumar, Design, simulation, and work function trade for DC and analog/RF performance enhancement in dual material hetero dielectric double gate tunnel FET, Silicon,14(15), (2022) 10101–10113. https://doi.org/10.1007/s12633-022-01765-w

[17] Dharmender, K. Nigam, Low-K dielectric pocket and workfunction engineering for DC and analog/RF performance improvement in dual material stack gate oxide double gate TFET, Silicon, 13, (2021) 2347–2356. https://doi.org/10.1007/s12633-020-00822-6

[18] Vedvrat, M.Y. Yasin, V. Gupta, D. Pandey, Improved Switching and Analog/RF Behaviour of SiGe Heterojunction Dielectric Modulated Dual Material Nano Silicon Tunnel FET for Low Power Applications, Silicon 16, (2024)1297–1308. https://doi.org/10.1007/s12633-023-02755-2

[19] Vedvrat, Assessment of Trap Charges for Analog/RF FOMs and Linearity Behaviour on InAs Based Dual Metal Hetero Gate Oxide TFET for Enhanced Reliability, Silicon, 16, (2024) 6107–6121. https://doi.org/10.1007/s12633-024-03137-y

[20] P. P. Goswami, R. Khosla, B. Bhowmick, RF analysis and temperature characterization of pocket doped L-shaped gate tunnel FET, Applied Physics A, 125(733), (2019) 1–12. https://doi.org/10.1007/s00339-019-3032-8

[21] S. Kumar, K. S. Singh, K. Nigam, V. A. Tikkiwal, and B. V. Chandan, Dual-material dual-oxide double-gate TFET for improvement in DC characteristics, analog/RF and linearity performance, Applied Physics A, 125(5), (2019) 353. https://doi.org/10.1007/s00339-019-2650-5

[22] K. M. C. Babu, E. Goel, Evolution of tunnel field effect transistor for low power and high-speed applications: A review, Silicon, 14(17), (2022) 11051–11060. https://doi.org/10.1007/s12633-022-01826-0

[23] K. Boucart, A. M. Ionescu, Double-gate tunnel FET with high-k gate dielectric, IEEE Transactions on Electron Devices, 54(7), (2007) 1725–1733. https://doi.org/10.1109/TED.2007.899389

[24] Vedvrat, M. Y. Yasin, D. Pandey, Optimization of dual material based dielectric modulated heterojunction double gate tunnel FETs with noise reduction analysis for high-frequency applications, Silicon, 16(9), (2024) 4061-4075. https://doi.org/10.1007/s12633-024-02987-w

[25] Z. Yi, Q. Shao, J. Zhang, Super tiny nanoscale graphene nanoribbon field-effect transistor, Chinese Journal of Physics, 59, (2019) 572–577. https://doi.org/10.1016/j.cjph.2019.03.015

[26] E. Goh, H. C. Chin, K. L. Wong, I. S. B. Indra, M. L. P. Tan, Modeling and simulation of the electronic properties in graphene nanoribbons of varying widths and lengths using tight-binding Hamiltonian, Journal of Nanoelectronics and Optoelectronics, 13(2), (2018) 289–300. https://doi.org/10.1166/jno.2018.2206

[27] Y. W. Son, M. L. Cohen, S. G. Louie, Energy gaps in graphene nanoribbons, Physical Review Letters, 97(21), (2006) 216803. https://doi.org/10.1103/PhysRevLett.97.216803

[28] B.R. Raad, S. Tirkey, D. Sharma, P. Kondekar, A new design approach of dopingless tunnel FET for enhancement of device characteristics, IEEE Transactions on Electron Devices, IEEE, 64(4), (2017) 1830–1836. https://doi.org/10.1109/TED.2017.2672640

[29] S. Kumar, K. Nigam, S. Chaturvedi, A. I. Khan, A. Jain, Performance improvement of double-gate TFET using metal strip technique, Silicon, 14, (2021) 1759-1766. https://doi.org/10.1007/s12633-021-00982-z

[30] I. Silvaco, ATLAS Device Simulation Software, Silvaco Int., Santa. Clara, CA, USA, Version 5.14.0.R, 2018.

[31] R. Saha, R. Goswami, and D. K. Panda, Analysis on electrical parameters including temperature and interface trap charges in gate overlap Ge source step shape double gate TFET, Microelectronics Journal,130, (2022) 105629. https://doi.org/10.1016/j.mejo.2022.105629

[32] W. T. R. W. Shockley, W. T. Read Jr, Statistics of the recombinations of holes and electrons, Physical review, 87(5), (1952) 835. https://doi.org/10.1103/PhysRev.87.835

[33] S. Tirkey, D. Sharma, B.R. Raad, D.S. Yadav Introduction of a metal strip in oxide region of junctionless tunnel field-effect transistor to improve DC and RF performance, Journal of Computational Electronics ,16(3), (2017) 714–720. https://doi.org/10.1007/s10825-017-1032-5

[34] R.K. Sachan, Vedvrat, S. Bajpai, Temperature Sensitivity Assessment of Nonlinear Channel Tunnel Field-Effect Transistor for Raised Efficiency

and Reliability in Nanoscale Electronics, International Research Journal of Multidisciplinary Technovation, 7(2), (2025) 261-276. https://doi.org/10.54392/irjmt25218

[35] S. Kumar, K. Nigam, S. Chaturvedi, A.I. Khan, and A. Jain, Performance Improvement of Double-Gate TFET Using Metal Strip Technique, Silicon, 14, (2022) 1759–1766. https://doi.org/10.1007/s12633-021-00982-z

Authors Contribution Statement

Sushroot: Conceptualization, Methodology, TCAD Software, Data curation, Analysis and Interpretation of data, Writing- Original draft preparation, Visualization, Investigation. Syed Hasan Saeed: Supervision. Vedvrat: Validation, revision and editing. Shrish Bajpai: Supervision. All the authors read and approved the final version of the manuscript.

Funding

The authors declare that no funds, grants or any other support were received during the preparation of this manuscript.

Competing Interests

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

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